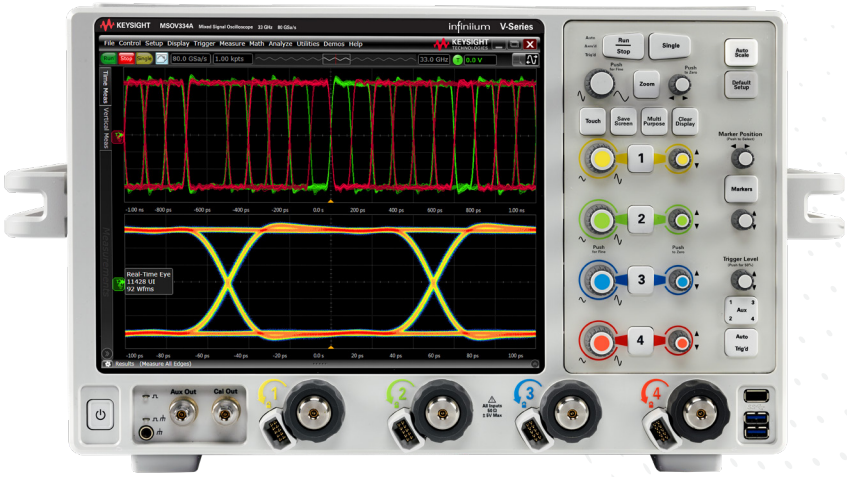
APPLICATION NOTE

Understanding PCI Express® 3.0 Physical Layer Transmitter Testing



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Overview

PCI Express® (PCIe®) technology has become the interconnect of choice for high-performance applications, including servers, peripherals, graphics,imaging, and storage I/O. Designers of PCIe systems and devices are faced with the demand for more reliable systems that can work with the exploding number of PCIe-based devices and the ever increasing demands to go faster.

The PCI and then the PCIe standard provide a way for multiple vendors to manufacture devices that can interoperate. The PCIe standard is on its 3rd generation with a 4th generation under development. PCI Express is a serial point-to-point, multi-lane interconnect between two devices, which means it communicates directly with devices via a switch that directs data flow.This allows for “hot swapping” or “hot plugging,” meaning cards in PCIe slots can be changed without shutting down the computer. It implements packet based protocol for information transfer. It also offers scalable performance based on 1 to 32 signal lanes implemented on the PCIe interconnect. Each serial link transfers data in one direction only and can be routed as a differential trace pair, relatively independent of the other links. Each receiver/transmitter pair is called a lane. Physical layer testing is done on each PCIe lane to support the critical need for standards compliance and interoperability.

As a broadly adopted standard, PCIe technology benefits from several decades of innovation with universal support in all major operating systems, a robust device discovery and configuration mechanism, and comprehensive power management capabilities that very few, if any, of the other I/O technologies can match. PCIe technology has a flexible, layered protocol that enables innovations to occur at each layer of the architecture independent of the other layers. PCIe technology is mature and compatible devices have been shipping for more than a decade. However, the need for robust testing for standards compliance is just as important as ever. These rigorous tests assure interoperability, reliability, and overall improved functionality from generation to generation.

The standards that comprise PCIe are managed by a non-profit organization called the Peripheral Component Interconnect Special Interest Group (PCI-SIG®). The PCI-SIG is run by a board of nine member-companies.

PCIe Benefits

High Performance	Low cost	Power management
– Low overhead – Full duplex, multiple outstanding requests – Scalable port width (x1 to x32) – Scalable link speed (2.5 /5.0 /8.0GT/s/per lane)	– High volume/ commodity – Can eliminate the host bus adapter (HBA) cost	– Direct attach to CPU can eliminate HBA power – Various low power levels (L0, L1, L2)

Background: PCIe Layers and Testing Requirements

Validating designs for PCIe device performance involves characterizing the reference clock and data signals. There are 3 different categories of testing required to reach compliance: physical layer, datalink layer, and interoperability. The different categories of tests are performed by different types of instruments.

1. Transmitter (Tx) test of the physical layer is validated by oscilloscopes
2. Receiver (Rx) test of the physical layer is validated by BERTs (bit error ratio testers)
3. Datalink layers are validated by a protocol analyzer

Figure 1 illustrates the different layers within the PCIe protocol and which of those layers apply to the different PCI-SIG test requirements. Products must successfully pass all tests at an official PCI-SIG workshop using approved test fixtures to be deemed compliant and branded as an approved PCIe device. Key parameters include rise-time, amplitude, eye width, jitter, and Tx phase-locked loop (PLL) bandwidth and peaking.

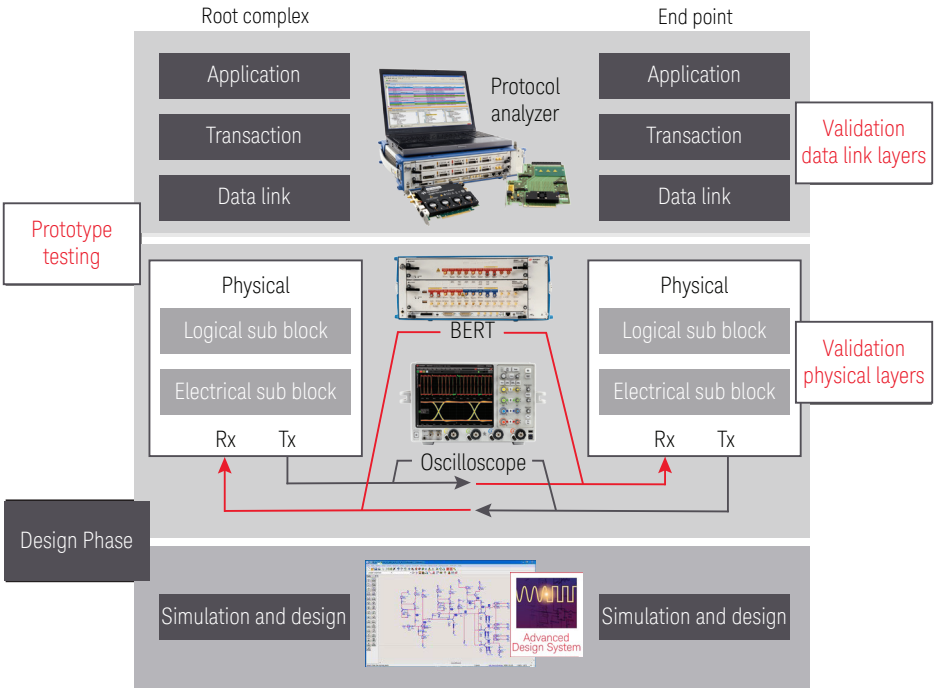
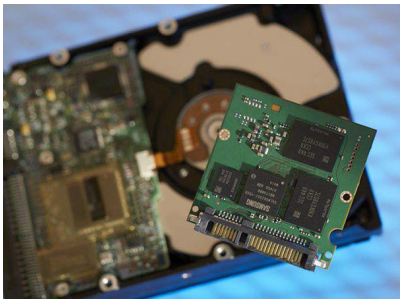


Figure 1. PCIe is a layered protocol, split between physical properties tested by oscilloscopes and BERTs and transaction/data link properties tested by protocol analyzers. The design simulation (represented at the bottom) should take into account all of the different testing requirements.

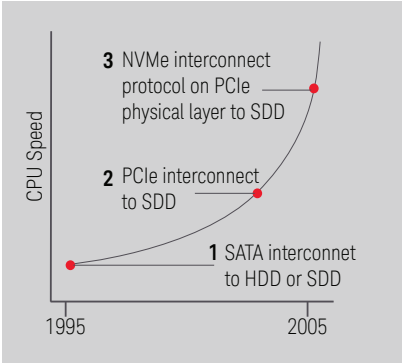
For the physical layer there are two different specifications approved by the PCI-SIG, the Base specification and the PCIe Card Electromechanical (CEM) specification. The Base spec defines electrical performance at the die-pad of the device; the CEM spec defines performance at the connector. The two specifications operate independently. The Base spec is used for testing at the chip, new silicon ICs for example, and has a larger set of tests that are run. For each of these specifications, physical layer transmitter and receiver testing must be done.

Eamples of use



PCIe technology is used by many different applications, one of the more popular is as an interconnect for storage. SSDs (solid state drives) provide a great example. They are quickly replacing traditional spinning hard-disk drives (HDDs) due to their superior reliability and speed. It is this transition that is motivating a move from SATA, SAS and SCSI to NVMe at the application layer of PCIe for storage applications.

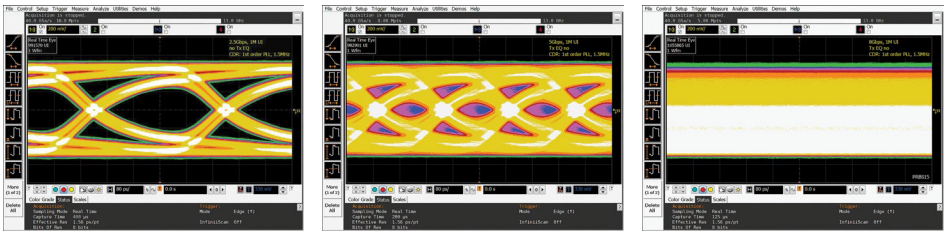
SSD interconnect history



1. SATA was used for many years as the serial bus to get data to the spinning hard disk drive (HDD). The read/write speed of the HDD was the speed bottleneck. With the introduction of SSDs, SATA became the bottleneck.
2. PCIe enabled faster data transfer to SSDs minimizing the bus as the bottleneck.
3. The NVMe implementation as the interconnect protocol running the PCIe physical layer allows the full speed potential of SSDs to be achieved physical layer to SDD

Challenge: Higher Speeds Require New Testing Methods

As the speed of PCIe has increased over multiple generations, it has started to suffer eye closure. This is due not only to the speed, but also the channel lengths supported which has an impact on how validation testing of the physical layer is done. You can see the impact of faster speed in the comparative receiver eye screen shots of Figure 2.



PCIe 1.0
2.5 GT/s receiver eye

PCIe 2.0
5 GT/s receiver eye

PCIe 3.0
8 GT/s receiver eye

Figure 2. PCI Express eye diagrams as speed has increased generation to generation. The eye diagram is smaller and smaller, resulting in less test margin.

With PCIe 3.0, 8 GT/s PCIe signals become a closed eye specification at the receiver pins. To enable correct communication, the Tx and Rx need to agree on what level will constitute a one and a zero, and employ a number of techniques to generate a clean eye. This agreement is done via link training and is tested with a variety of methods including equalization and de-emphasis. These tests were added for PCIe 3.0 and are critical for success in 8 GT/s PCIe 3.0 and above.

This application note focuses on transmitter testing of PCIe technologies. For a more indepth understanding of the Rx and protocol-level testing and validation processes and challenges, see 5992-0818EN Understanding PCI Express® 3.0 Physical Layer Receiver Testing and 5992-0865EN Data Link and Transaction Layer Testing for PCI Express® & NVMe™.

PCIe 3.0 Tx testing challenges

- Manual lane-to-connection of test signals with fixtures
- Measurement at receiver pins will show a closed eye. How can you see what the receiver is seeing inside the chip?
- The oscilloscope can:
  - Perform equalization on acquired PCIe 3.0 signals to show what the receiver is seeing internally The application includes CTLE and DFE models.
  - De-embed cables and test fixtures to minimize the impact these have on measured results.
- Complexity of compliance software
- Clock and Data recovery tests (CDR)
  - Reference clock phase jitter filters for dual port system measurement
- Base specification tests for measuring IC transmitter outputs (uncorrelated jitter, etc)

PCIe Tx Test Requirements

Testing for any PCIe specification requires a real-time oscilloscope with electrical test software for compliance and validation. Official compliance testing is performed at PCISIG workshops on systems (motherboards) and add-in adapter cards. Passing the compliance tests is a requirement for vendors to be included on the PCI-SIG integrator's list and to use the PCIe logo. Many vendors will want to test their product before attending a PCI-SIG workshop.

With PCIe 3.0, there are a number of specific challenges related to transmitter validation.

Manual connector & fixture changes during testing

During the CEM specification process, the tester must physically connect each lane of the device under test to the test equipment, one at a time. To emulate the worst case scenario, the specification requires maximizing the effects of crosstalk on eye closure. To do this, it is necessary to terminate all unused lanes to 50 ohms. Therefore, when switching from lane to lane, the tester must switch not only cables but also terminations. Removing and/or replacing terminators is both tedious and time consuming. The Tx setup also involves multiple test conditions for the DUT's transmitter. This process can be time consuming. Using a switch matrix, teams can automate the process to run with minimal user assistance.

De-emphasis

For PCIe 3.0, a large number of transmit de-emphasis states were added. De-emphasis compensates for loss through the channel. At the transmitter side, de-emphasis is done by shaping signals with boosted higher-frequency content. This boosting is attenuated in the channel. All appropriate levels of Tx de-emphasis for endpoints and necessary presets must be tested. These PCIe 3.0 requirements give the transmitter greater flexibility to drive a level of de-emphasis that more appropriately accounts for the step response of the channel to which it's connected.

De-embedding

Another contributor to eye closure is fixtures and cables used for testing. De-embedding is a process to first measure the loss associated with the channel, probe, cables or fixture and then 'subtract' that value out of the final DUT measurement and is accomplishedusing S-parameters.

Rx equalization: See the eye inside the chip

Reference receiver equalization was also added with the introduction of the PCIe 3.0 specification. With the 8 GT/s speed of the PCIe 3.0 specification, the eye is closed at the receiver pins. Equalization is one of the methods used to open the eye up.

Receiver equalization is a process that uses the combination of continuous time linear equalization (CTLE) and decision feedback equalization (DFE) to account for the ISI and open the eye so the receiver can see the signals sent from the transmitter.

As transmitter signal rates increase, the channel the signals travel through attenuates higher frequencies. This is known as channel insertion loss. This distortion can cause a partially or completely closed eye at the receiver pins. The CTLE is a frequency domain filter that provides frequency response correction. Its purpose is to filter serial Rx input data to “boost” high frequency content attenuated in the channel. Inter-symbol interference distorts the signal causing eye closure. This is addressed with a DFE filter to subtract out channel impulse responses of previous data bits to zero-out ISI contributions on the current bit.

PCIe standards do have reference equalization but do not specify the implementation. Any user-defined implementations that are equal or better to the reference are acceptable.

Figure 3 shows a signal path through the channel requiring equalization to open the eye, and channel insertion loss. Serial data equalization tools provide fast and accurate equalization using Feed-Forward Equalization (FFE), Continuous Time Linear Equalization (CTLE) and Decision Feedback Equalization (DFE) modeling in real time. The tool allows you to use a combination of the equalization, which is found in actual designs. Serial data equalization software allows you to input your own equalizer settings and tap values that are used in your design, allowing you to simulate the eye opening in your receiver. If you prefer, the software can find the optimal tap values for you as well, which you can use as reference for your designs.

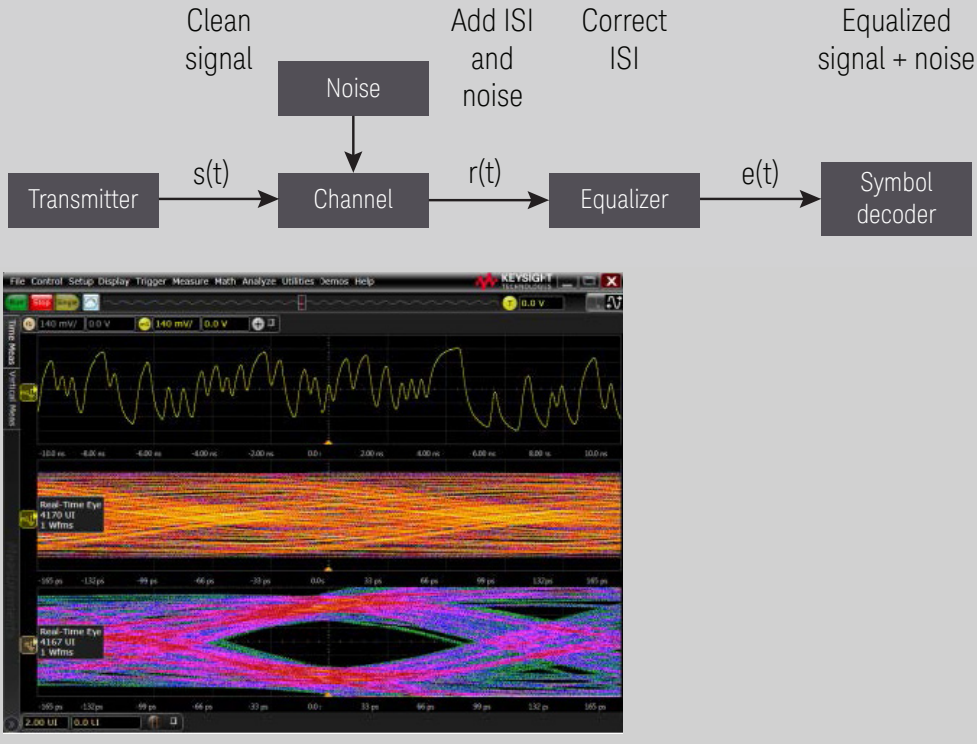


Figure 3. Serial data equalization opens the closed eye using CTLE and DFE methods.

Complexity of compliance software

Transmitter tests are done by connecting the device under test (DUT) to a test fixture and probing the SMA connectors on the test fixture. For CEM specification test, the set of tests defined by the PCI-SIG and designed to test all aspects of the PCIe standard are collected together in a software package called SigTest. SigTest is available from the PCI-SIG and is the software package that is used for all PCIe electrical testing at compliance workshops. The SigTest software generates PCIe patterns on a host that are used to determine signal quality. An oscilloscope running the PCIe compliance software makes measurements on the data rate, unit interval, jitter, and eye diagrams for both transition and non-transition bits. The scope's PCIe compliance application generates a summary test report that shows overall pass/fail, data rate, jitter, and eye diagrams.

In addition to passing the SigTest signal quality tests, which are run within your oscilloscope vendor's software application at the compliance workshop events, the PCI-SIG requires that PCIe systems and add-in adapter cards also pass a rigorous suite of electrical transmitter compliance tests. For CEM specification compliance only, designers must perform these tests before attending the compliance workshop events[1].

Most of the difficulty in implementing these tests comes from the instrumentation setup, probe calibration and capture, and analysis of the pass/fail results with respect to the limits specified. The use of validation and compliance software, however, integrates and automates testing of all PCIe specifications. There are different compliance patterns, tests and limits required for each PCIe generation.

Planning ahead

With less test margin for error due to the higher speeds, the need for accurate simulations in the design phase becomes more important. As all developers know, good simulation in the design phase can help to alleviate problems that might appear further down the design cycle. Testing compliance before committing to the build of prototypes can save time and money. Obviously it is much easier to change the design model and determine the consequences than it is to revise the chip. Simulation and then assessing if your prototype meets your simulation becomes a vital component as the validation testing requirements are more challenging to meet (Figure 4).

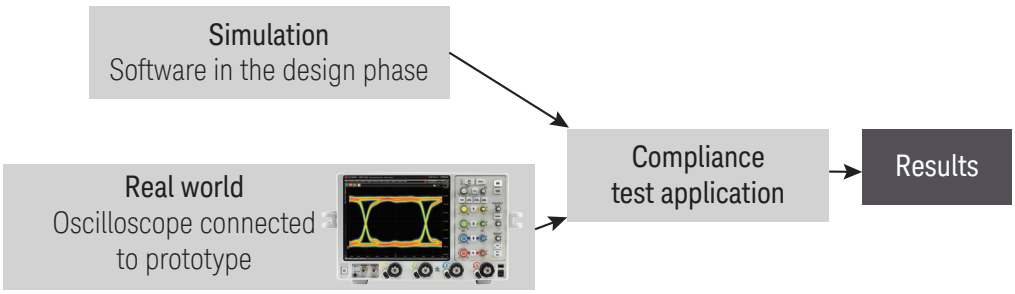


Figure 4. The simulated design with appropriate loading can be compared to the actual scans of the prototype to ensure the system is working as expected.

1. These tests are published on www.pcisig.com and are available as test assertions in the PCIe Base Specification for 1.x, 2.x, and 3.x.

PCIe version	1.0a	1.1	2.0	3.0	4.0
Data transfer rate	2.5 GT/s	2.5 GT/s	5.0 GT/s (2.5 GT/s)	8.0 GT/s (2.5 & 5.0 GT/s)	16.0 GT/s (2.5, 5.0 & 8.0 GT/s)
Data fundamental frequency	1.25 GHz	1.25 GHz	2.5 GHz	4.0 GHz	8.0 GHz
Data encoding	PRBS 16 scrambling and 8b10b coding	PRBS 16 scrambling and 8b10b coding	PRBS 16 scrambling and 8b10b coding	2.5 and 5 GT/s: PRBS 16 scrambling and 8b10b coding 8 GT/s: PRBS 23 scrambling and 128b130b coding	2.5 and 5 GT/s: PRBS 16 scrambling and 8b10b coding 8 and 16 GT/s: PRBS 23 Scrambling and 128b130b coding
Total bandwidth for x16 link	~6.4 GB/s	~6.4 GB/s	~12.8 GB/s	~25.6 GB/s	~32 GB/s
Key changes	– Initial release	– Tighter jitter and reference clock tests	– Speed – Cable specification – PLL bandwidth test – Tighter jitter and reference clock tests – New de-emphasis levels	– Speed – Higher PLL bandwidth – More complex de-emphasis – PRBS 23 scrambling	– Speed – Shorter channel – Single connector – More transmit deemphasis states – More taps on DFE – Much smaller RX eye height.
Physical layer test requirements	Tx	Tx	Tx, PLL	Tx, PLL, Rx	Tx, PLL, Rx

Table 1. Comparative table between different versions of PCIe specification.

PCIe 4.0

Currently, the PCI-SIG is focused on developing the fourth generation of PCIe and their efforts have been divided into different work groups. One of those groups works on the electrical part of the specification, which defines the electrical characteristics of the SerDes (serializer/deserializer), drivers, receivers, and equalizers. Another work group is focused on protocol including the link, and transactions. The resulting work of the combined groups will come together and are referred to as the Base specification for PCIe 4.0, which defines the physical card link layer requirements for a PCIe component or device.

PCIe 4.0 is planned to be backward compatible with earlier generations of PCIe. Therefore, a first-generation device will be able to plug into a PCIe 4.0 system (and vice versa). Backward compatibility has been a core requirement within PCIe thus far in its evolution.

Many of the things for PCIe 4.0 are trending to be the same as they were for PCIe 3.0. To accelerate from 8 GT/s (3.0) to 16 GT/s (4.0), every advantage from the previous generation will have to be pushed even further. This includes Rx equalization as well as using statistical techniques to analyze channel compliance.

The major breakthroughs of 3.0, such as encoding the 8 b/10 b to 128 b/130 b (which afforded a 20% performance improvement), are not applicable for the 4.0 release. Achieving PCIe 4.0's target of 16 GT/s will require the cumulative effect of many smaller adjustments across most elements of the PCIe transmitter, channel, and receiver transmission line specifications in order to be successful.

Another key difference between PCIe 3.0 and 4.0 will be the length of the channel. PCIe 3.0 was designed to operate with a maximum 50 cm (20 inch) channel with two connectors, supporting a 20 dB of loss at Nyquist (4 GHz). For 4.0, the Nyquist frequency will increase to 8 GHz, which subsequently causes additional insertion loss. Without any other mitigating technology, the channel length for 4.0 is going to be significantly shorter and will likely support only one connector.

Keysight Solutions

Keysight solutions for PCIe technology span from design simulation through physical layer, to protocol test. Keysight continues to be an active participant in the PCI-SIG group to ensure coverage for future generations of PCIe technology. In addition to test solutions, Keysight's skilled application engineers with access to PCIe experts can help you with your PCIe test challenges.

Keysight's Infiniium V-Series oscilloscopes (Figure 5) provide industry-leading accuracy that ensures greater insights in analysis and debug of high-speed designs. This is especially important with the high serial speeds of PCIe and the decreased margin that these speeds impose.

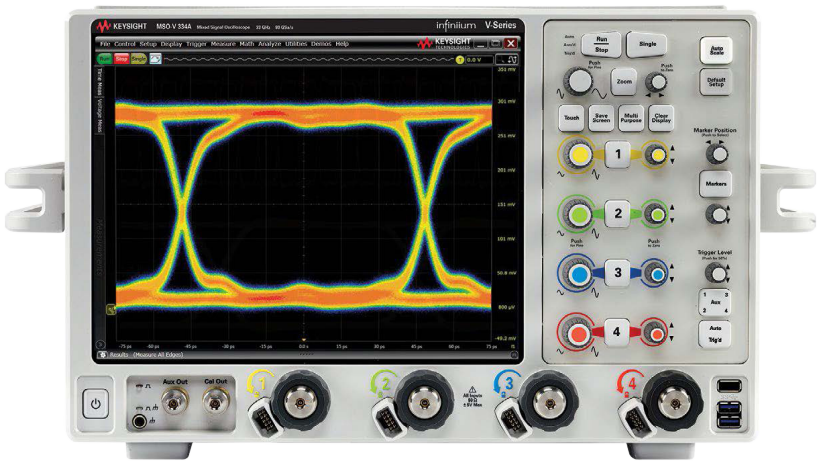


Figure 5. The Infiniium V-Series comes in 8 - 33 GHz DSO, DSA, and MSO oscilloscope models that provide superior measurement accuracy, enhanced analysis tools and advanced probing systems.

Ininiium V-Series oscilloscopes incorporate innovative technology designed to deliver superior measurements. The 12.5 Gb/s, industry's longest 160-bit hardware serial trigger and world's fastest 20 GSa/s digital channels provide timely validation and debug. The 160-bit sequence length is more than sufficient to trigger on the longest symbols in PCI Express 3.0, 130 bits. If the trigger bit sequence is insufficient, you will not be able to reliably trigger on an event you want to identify, making the debug process more challenging.

The V-Series can decode the data packet at the PCIe 3.0 application level, providing deeper protocol insight into the application. When there's an error, designers can now go in and debug the issue at the physical layer (where the signal integrity is corrupted) or at the protocol layer (where the data is incorrectly transmitted). Designers can use the same oscilloscope for everyday debugging to perform automated testing and margin analysis based on the PCI-SIG specified tests.

Keysight's N5393D PCI Express electrical performance validation and compliance software provides a fast and easy way to verify and debug PCIe designs (Figure 6). The PCIe electrical test software allows for automatic execution of PCIe electrical transmitter tests, and displays results in a flexible report format. In addition to the measurement data, the report also provides margin analysis that shows how closely a device passed or failed each test.

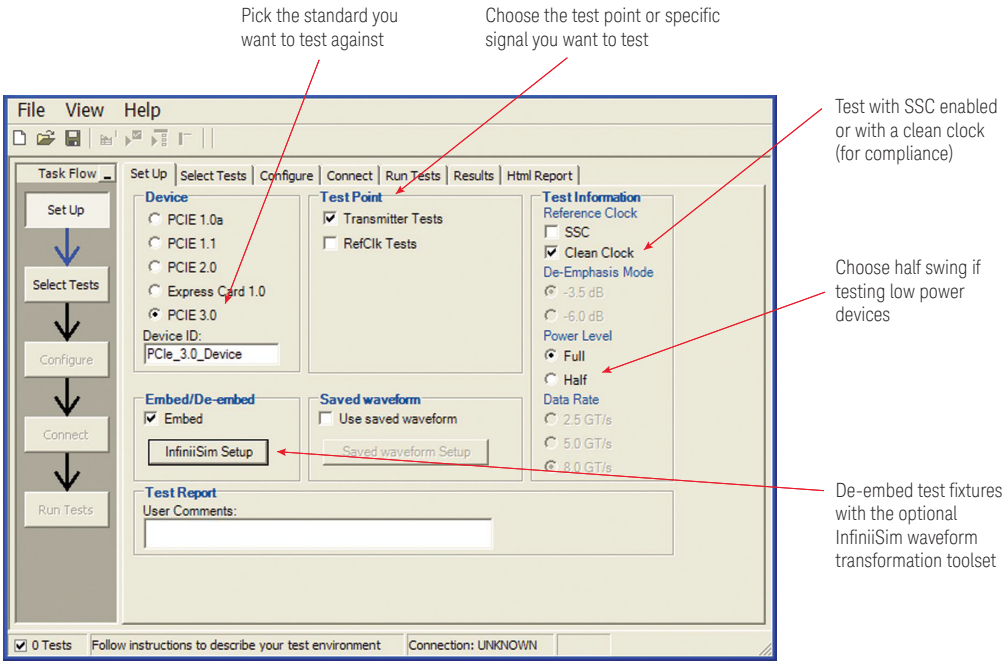


Figure 6. The software allows you to easily specify the test standard to use to test the compliance of your device. This makes test setup easy as only the appropriate tests for the test point you pick are shown on later test selection pages.

For PCIe 3.0 measurements, Keysight's N5393D software automatically calculates uncorrelated total jitter, uncorrelated deterministic jitter, and uncorrelated pulsewidth jitter necessary for validating new PCIe 3.0 compliant chipsets.

The PCIe electrical test software includes a test for verifying that the transmitter is compliant with the PCIe 3.0 specifications at 8 GT/s for both silicon validations (as per the PCIe Base specification) as well as for add-in cards and motherboard systems (as per the PCIe CEM specification) and PCIe reference clocks. The base specification defines electrical performance at the die-pad of the device; the CEM defines performance at the connector. The Keysight N5393D software tests both.

In addition to supporting PCIe 3.0 measurements, the PCIe electrical performance validation and compliance software performs a wide range of electrical tests as per the PCIe 1.0a, 1.1[1], and 2.0 electrical specifications for new silicon, add-in cards, and motherboard systems as documented in section 4 of the base and CEM specifications as well.

1. For versions of devices compliant with PCIe 2.0 or earlier, random jitter is also reported for completeness and a voltage margin "eye" diagram is included in the final HTML report. DJ and TJ values are specified in the PCIe 2.0 specification and are required for compliance verification.

Keysight offers a complete line-up of software tools to help you verify your PCIe 3.0 Tx design:

Switch matrix software tool, the Keysight N5393D Option 7FP for the PCI Express compliance application, used together with switch matrix hardware, enables fully automated testing for this multi-lane digital bus interface.

Clock recovery and eye diagram analysis through serial data analysis/mask testing software, E2688A, recovers embedded clocks and enables eye masks and measurements.

Serial data equalization software (SDE), N5461A (Figure 7), provides fast and accurate equalization using Feed-Forward Equalization (FFE), Continuous Time Linear Equalization (CTLE), and Decision Feedback Equalization (DFE) modeling in real time. Serial data equalization software allows you to input equalizer settings and tap values from your design, enabling simulation of the receiver eye opening. If preferred, the software can also find the optimal tap values, which can be used as references for your designs.

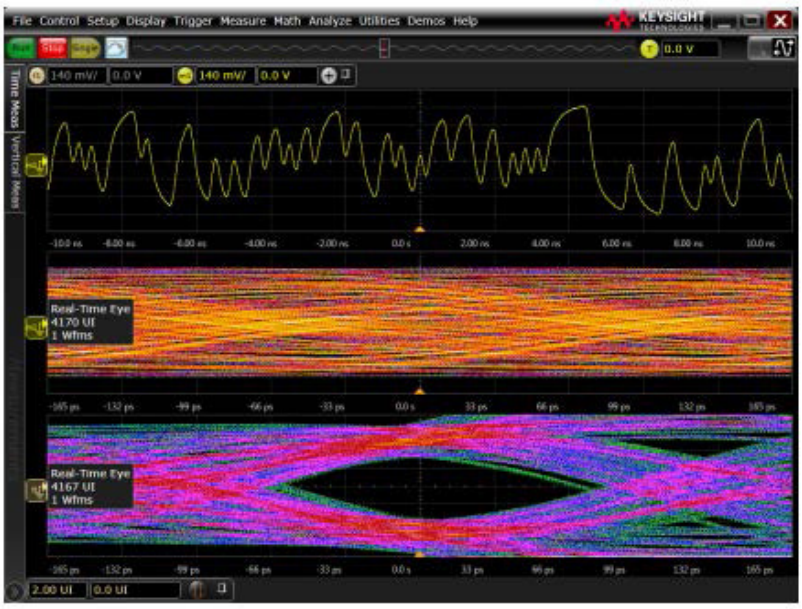


Figure 7. Serial data equalization software.

Jitter analysis software, N5400A EZJIT Plus, automatically detects embedded clock frequencies and repetitive patterns of the data on the oscilloscope inputs and calculates the level of data-dependent jitter (DDJ). Get advanced decomposition, analysis and views of jitter necessary for fast and accurate insight into your signal. Decompose jitter into components, view BER bathtub curves and estimate TJ at low BER. Whether your signal is subject to channel ISI, power supply interference or crosstalk from adjacent signal paths, EZJIT Plus enables you to accurately estimate TJ and determine the sources of jitter affecting your signal.

Keysight gets involved, you benefit

Keysight's solutions for digital applications are driven and supported by Keysight experts that are involved in the various international standard committees. We call it the Keysight Digital Test Standards Program. Our experts are active in the Joint Electronic Devices Engineering Council (JEDEC), PCI Special Interest Group (PCI-SIG®), Video Electronics Standards Association (VESA), Serial ATA International Organization (SATA-IO), USB-Implementers Forum (USB-IF), Mobile Industry Processor Interface (MIPI) Alliance, and many others. Our involvement in these standards groups and their related workshops, plugfests, and seminars enables Keysight to bring the right solutions to the market when our customers need them.

De-embed the probe, cable or fixture through InfiniiSim, an application that allows the user to probe at one point, and determine what the waveform is at a different point. Convert, or filter, an acquisition to portray a waveform at a different circuit location or different circuit rendering than where probed. It works by relating the transfer functions of two circuits to yield an overall transfer function between them. The two circuits (the 'measurement circuit' and 'simulation circuit') are defined by the user. The measurement circuit represents the measurement setup the user has on the bench, while the simulation circuit represents the circuit the user would like to have. InfiniiSim can de-embed fixtures or cables or switch networks that are placed between the oscilloscope and the device to be measured and help to view waveforms in physically un-probable locations. This highly-configurable tool enables engineers to quickly do these things on their tool of choice, the oscilloscope.

Design simulation software, Keysight's Advanced Design System (ADS), enables end-to-end simulation of the physical layer (transmit, receive, channel, etc.) and leverages a unique position as a vendor of leading electronic measurement equipment and a provider of design simulation software. The user can start with an example schematic design from the W2352EP PCI Express Compliance Test Bench within ADS, and customize it to reflect their desired IP-block choice, channel design and connector selections. The PCI Express Compliance Test Bench writes out the simulated electrical and timing waveforms to file, in a format that Keysight's N5393D PCIe electrical performance validation and compliance software uses for offline or stored data. ADS and the W2352EP PCI Express (PCIe) Compliance Test Bench (Figure 8) help solve the problem of simulation-measurement correlation. If the simulation passes, designers can fabricate with confidence. When the prototype comes back from fab it can be plugged into the physical test bench for measurement using the exact same application to determine electrical and timing compliance. Where discrepancy occurs, it can be limited to the space between simulation and physical creation because the compliance application is identical in both cases.

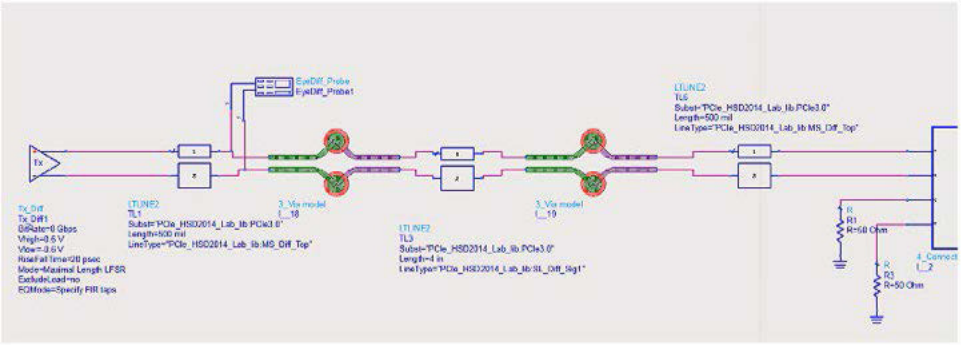


Figure 8. PCIe Gen 3 compliance test bench schematic of the transmitter side.

The PCI Express Compliance Test Bench product itself is available from within ADS and consists of two parts: the simulated test bench, and the waveform bridge script. The simulated test bench is composed of sub-circuits, namely a PCIe transmitter, a channel, and a PCIe receiver. Once the simulated test bench has been adapted to reflect your pre-manufacture design, the channel simulation runs, and writes the appropriate waveforms to the dataset. The waveform bridge script is a post-processing step that takes waveforms in the data set and writes them to a file that the N5393D Infiniium compliance test application can parse. This application can run on live data on the oscilloscope, as well as stored ("offline") data. In addition, you can run the application in "remote" mode, meaning that it can run on any Windows PC (including the one you run Advanced Design System on). In this way you can be assured that the tests you run on the pre-manufacture design simulation will be identical to the ones you will run when the prototype is subsequently manufactured.

Summary

PCIe has become the high-performance interconnect of choice for many types of I/O applications including graphics, networking and attached storage. While the evolution of PCIe for the current generation has brought greater speed, technical innovations have also introduced some new challenges in terms of transmitter testing and receiver testing according to the PCIe standard.

PCIe 3.0 devices' higher speeds simultaneously brought additional eye closure due to the channel lengths supported. This problem will continue with the upcoming release of PCIe 4.0, and will be coupled with the challenge that the channel will be shortened from the previous generation.

To accurately view the transmit data and analyze its signal fidelity, more complex clock recovery and jitter measurement techniques are now required. Real-time oscilloscopes with electrical test software for compliance and validation, along with simulation software that can take into account test requirements for validation, are necessary tools. This enables test and validation of PCIe designs to PCI-SIG compliance standards – thus ensuring reliability, interoperability, and overall functionality of current (PCIe 3.0) and future (PCIe 4.0) generations of PCIe-based designs.

Learn more at: www.keysight.com

For more information on Keysight Technologies' products, applications or services, please contact your local Keysight office. The complete list is available at:
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