APPLICATION NOTE

Overcoming Test Challenges of USB Type-C

The USB Type C connector is low profile and enables high speed data transport, orientation independent connection, sophisticated power management capability, high charging current capability and comes with system features that allow for broad use. Though the primary target market for the new connector is for mobile applications such as mobile phones and tablets, it can be used for desktop products as well as consumer electronics. The USB Type-C specification defines a 24 pin interface as well as silicon structure functionality in devices using it which aid discovery, power delivery configuration, and reconfiguration of the interface to use other digital transport protocols.

This application note provides an introduction to the USB Type-C connector, the interface functions it provides, test implications engineers face when integrating the connector into their designs, as well as recommended test solutions. You will also learn practical tools and techniques to address the many test parameters and evolving standards for design and test engineers using oscilloscopes to test and characterize USB Type-C designs.

KEYSIGHT TECHNOLOGIES

Introduction to the USB Type-C connection

The USB Type-C connection addresses connector Standards needs for USB 2.0 through 3.1, Thunderbolt, MHL, DisplayPort and more, for use in a broad range of applications. The slim, flippable connector enables USB to achieve newly defined USB3.1 data rates of 10 Gbs, with 40 Gbs within reach for two lane operation, which adds to the attractiveness of using the high performance Type-C connector. Handsets and devices including tablets, laptops and mobile phones will take full advantage of the smaller low-profile, powerful and reversible connector. The combined capability, power improvements and ease of use result in a complex system for design and test engineers.

An understanding of the USB Type-C connector structure will help to demonstrate the full potential of its capability and ease of use, as well as the complexity for test. The symmetrical pin configuration enables the connector to be rotated 180 degrees and still connect to like pins. For example, in Figure 1, the TX2 and RX2 connections shown in green, can be rotated and will connect where TX1 and RX1, shown in blue, are located. This makes it easy to engage the Type-C connector in either direction and provides orientation independence. The RX1 &TX1, and RX2 & TX2 provide two pair of differential lines, one for transmitting data and the other for receiving data, and offer up to 20 Gbs in data transmission speed per lane.

The power pins, four for VBUS and four for GND, manage up to 5 Amps which presents more challenges for cable and interconnect designs. The SBU1 and SBU2 pins are side band communication channels and provide additional connections and use for protocols other than USB.

The USB Type-C specification, which uses RX/TX pair for high speed transmission, also includes a simultaneous link of USB 2 (D+, D-) which can be used for standard USB 2 operations or as a supplemental link providing information for power delivery. The D+ connections are tied together, as are the D- connections to maintain the orientation independence of the connector.

The CC1 and CC2 lines manage the definition of the connector interface by providing three functions; orientation configuration management, supply power to cable and communication channel for power delivery.

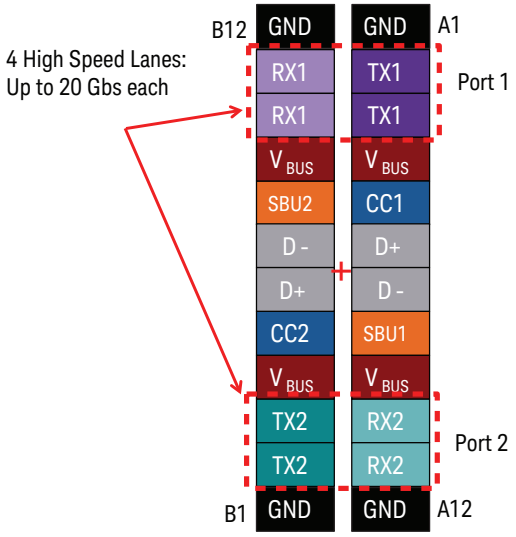


Figure 1. USB Type-C connector signal plan.

A USB Type-C device, using both USB 3.1 and 2.0 links, will use one of the RX/TX pairs (shown in blue and green in Figure 2) through a switch or port multiplexer (mux).

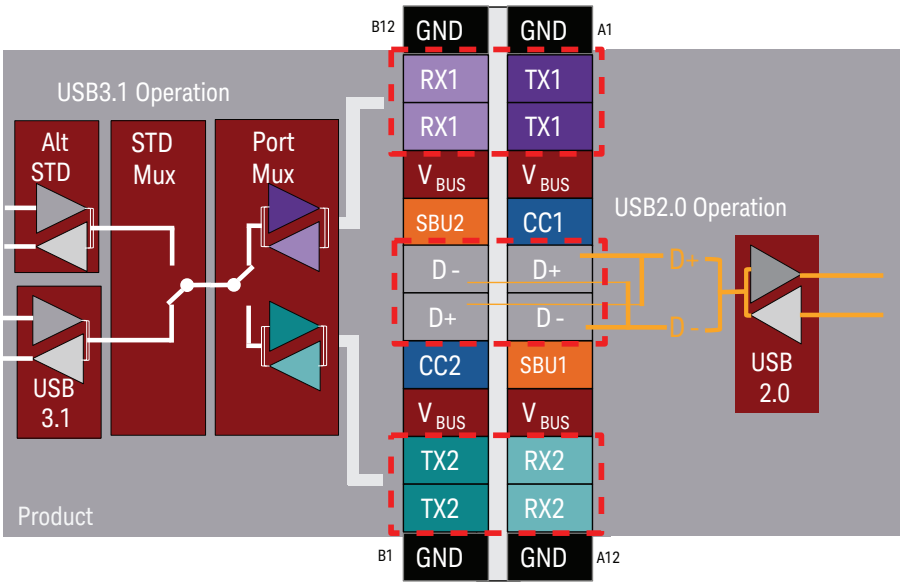


Figure 2. Host connection to a device using one RX/TX pair determined by the cc lines.

In this example, the USB 3.1 differential communications link is established through port 1 (blue connections). If the connector were flipped, the communications would be established through the port 2 (green connections). The USB 2.0 link uses the designated D+ and D- connections for a half-duplex link.

There are four VBUS power lines supporting up to 5 Amps at 20 V. In addition to adjustable power, the added intelligence of the USB Type-C connector enables it to negotiate the power direction. In other words, a device can switch from consumer to provider using the USB Type-C connection. For example, the supply can generate and provide power to the link partner, or if the supply decides to charge, it will initiate a contract with the link partner to have it provide the power. The power negotiation is a very important feature of the USB Type-C definition.

USB Type-C alternate mode protocols, such as DisplayPort, MHL and Thunderbolt use the SBU1 and SBU2 “sideband” signals to define functionality outside of standard USB 3.1 communications. DisplayPort uses SBU1/2 connections as AUX+ and AUX-. MHL uses them as e-CBUS for link discovery, link management and clock. Thunderbolt uses them as low speed RX/TX lines. The flexibility of the USB Type-C SBU1/2 lines enables the use of the connection for protocols other than USB.

The CC1 and CC2 pins are used to establish connectivity between a host and device regardless of the orientation of the cable. The USB Type-C connector maintains a host-to-device logical relationship even though it is reversible using a single-wire orientation detection. A cable has only one wire (simply referred to as the CC line) to make the connection between CC pins of host and the CC pins of a device. When the cable is plugged into the receptacle, the wire connects from CC of the receptacle to either CC1 or CC2 on the other end which determines the cable orientation. In Figure 3, CC1 is connected to both the host (downstream facing port) and the device (upstream facing port) with sense lines monitoring both link partners, recognizing that they are connected. The CC2 connection is terminated with the resistance RA, as specified, and provides a local power of +5 V where it is repurposed as V_{Conn} to power active cables.

When CC1 is connected between the up and downstream devices, TX1/RX1 (shown in blue in Figure 4) is used as the main high speed signal path from one device to the other and then to the port mux where it transmits data.

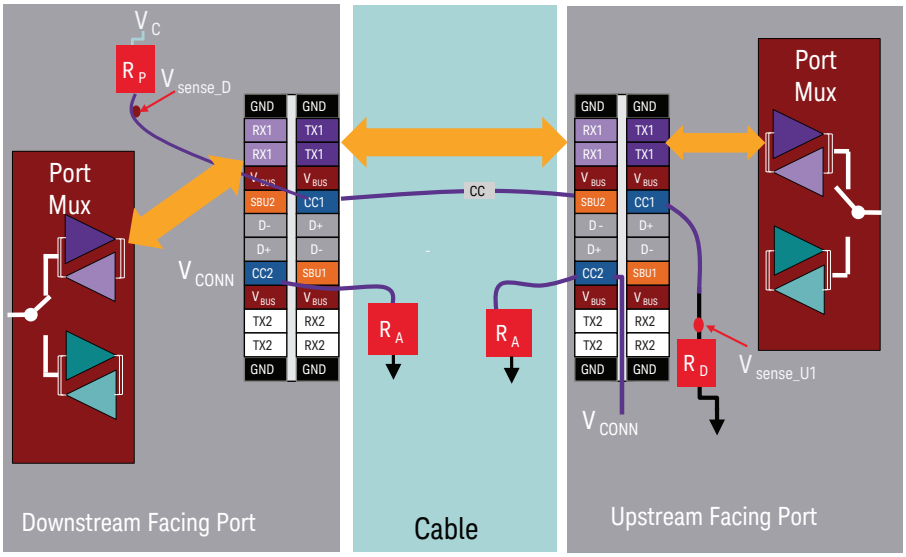


Figure 4. USB Type-C link with CC line terminations and data path multiplexers of host and device.

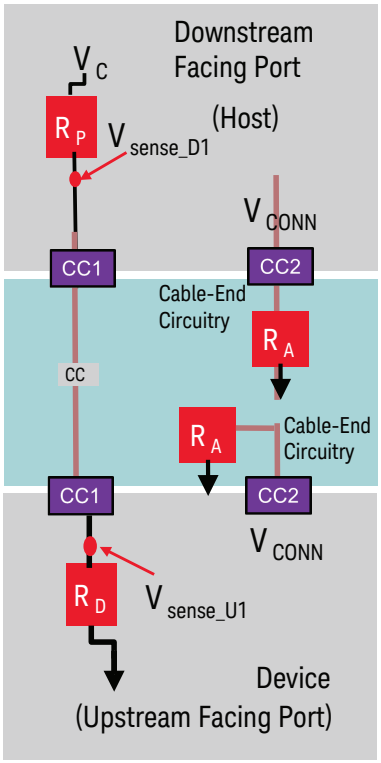


Figure 3. Host, cable and device connection uing one cc wire to connect the port 1 RX/TX pair.

If the cable connection is rotated or “flipped”, data would travel from TX1/RX1 in the downstream facing port (host) to the TX2/RX2 port of the device as shown in Figure 5. Also shown in Figure 5 is a connection for power delivery, which could be used to power a display for example, and is activated through the CC link. Power delivery, including voltage and current levels, and provider or consumer, are determined using the CC link.

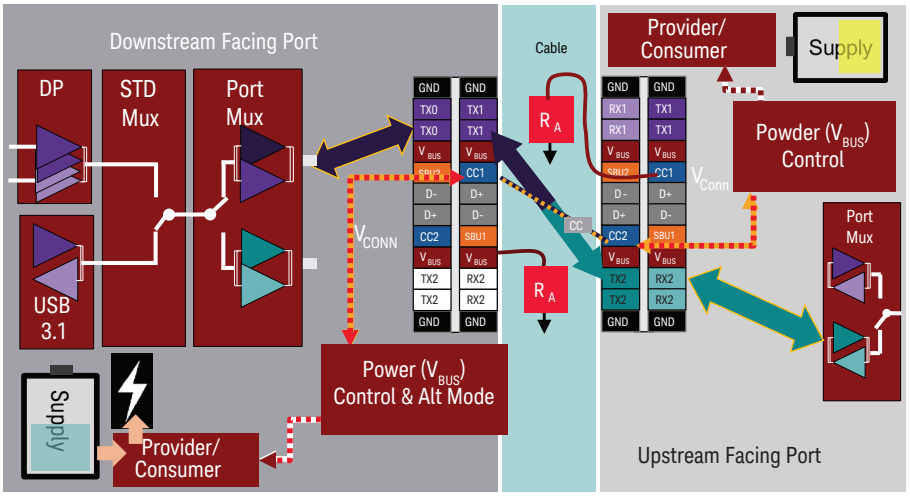


Figure 5. USB Type-C link illustrating a cable ‘flip’ and data routing.

The Type-C Alternate mode for DisplayPort uses all four RX/TX pairs and the SBU1/2 lines. Figure 6 shows an example of the Alternate mode for DisplayPort.

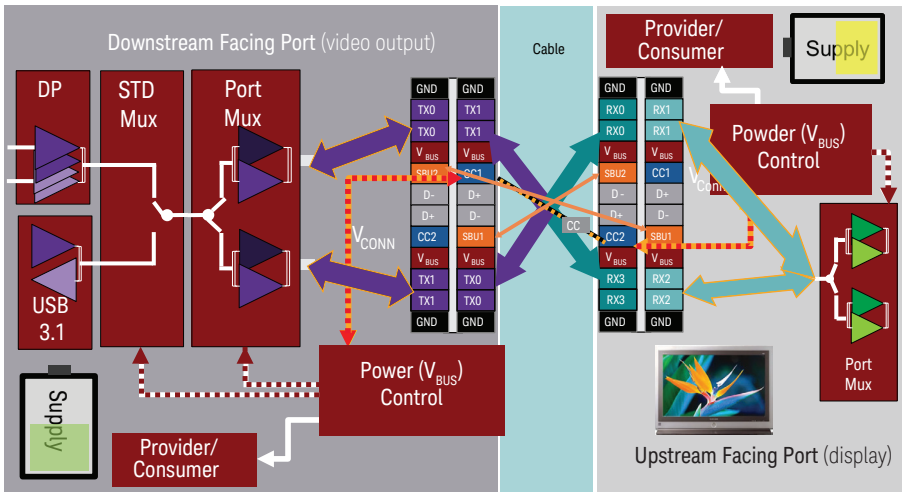


Figure 6. USB Type-C link with DiplayPort source (left) transmitting through a flipped cable to DisplayPort sink.

The additional capabilities of the USB Type-C connection will enable many more devices to take advantage of the powerful, flexible features this USB connection has to offer. Connecting between devices will be even easier for users, as they can plug it in in either direction and be allowed to connect more devices with multiple functions. However, when considering the validation engineers tasks for performing test validation of the devices, the job is more complex and has increased from just USB tests to include USB 3.1 on both ports since the cable can be flipped, USB 2.0, Power Delivery, and any Alternate mode(s) test regimens.

USB Type-C Test Challenges

For USB Type-C device test, the features, functions and capability requiring test validation include:

- USB and DisplayPort signals analyzed with a high bandwidth oscilloscope - Thunderbolt over type-C will require even higher bandwidth for analysis
- Test of both TX1/RX1 and TX2/RX2
- Test of all protocols that will be transmitted
- Ability to control CC signal loading (RP, RD, and RA) for power up , debug and test
- Ability to communicate over CC line for
  - Power setup: VBUS as consumer/provider, voltage and current settings
  - Alternate mode (protocol) control
- Ability to test the Power Delivery communication channel, its protocol and the VBUS profile including high current states
- Driving SBU1 and SBU2when an alternate mode is used

Many more tests and configuration considerations are needed to ensure devices meet the new USB Type-C standards, and when used, alternate protocol standards as well. By grouping these tests into Power Delivery, TX, RX, and cable/connector categories we can take a closer look at test implications and solutions. Engineers who are armed with the tools and techniques for USB Type-C testing will progress more quickly towards successful, accurate test results.

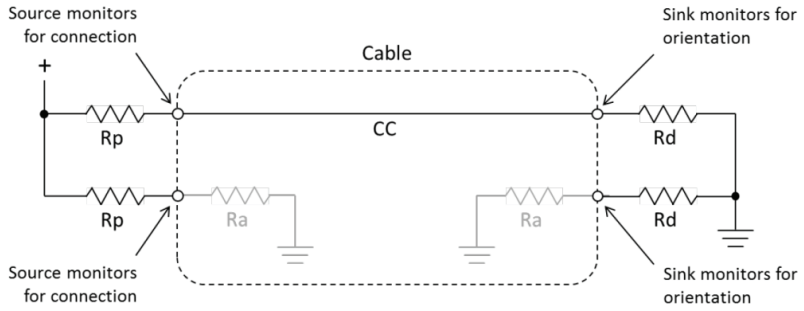


Figure 7. USB Type-C basic implementation.

Figure 7 shows the CC connection between the Rp source or “host” and the Rd sink or “device”, which is what we have historically learned to expect from a USB connection. In a more detailed diagram (Figure 8) you will see the host and device as dual role ports (DRP) which is aligned with the USB Type-C environment where the “host” and “device” roles can be swapped. The state of a DRP, whether it is acting as a “host” or a “device” at a given time, is managed by the CC line as a part of the PD infrastructure. Debug of the PD protocol is one of the biggest challenge engineers face since it requires access to the CC lines and the VBUS signal in order to be properly characterized. USB PD has specified voltage/current (power) levels that devices can select for operation making the ability to test PD levels as devices initialize very important.

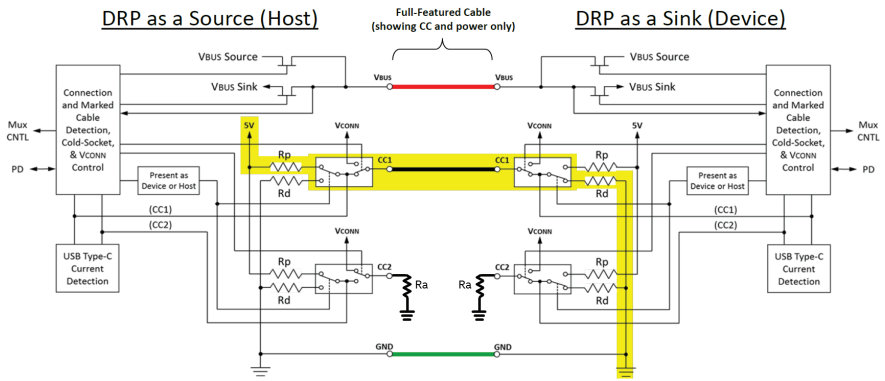
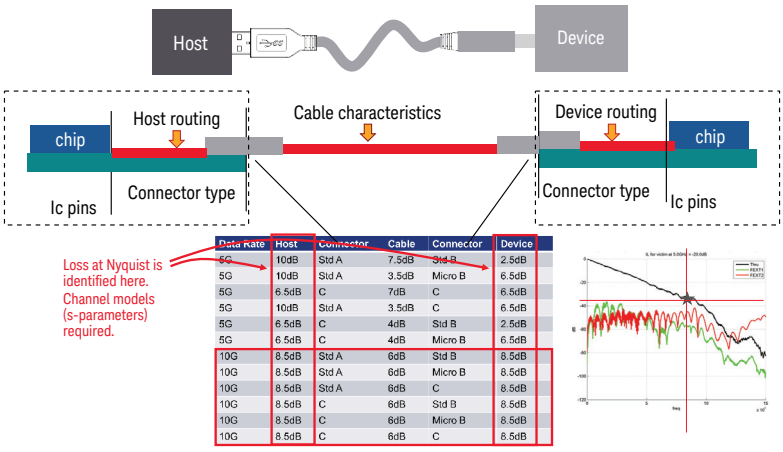


Figure 8. USB Type-C full feature implementation.

The USB-PD protocol is still evolving and there are a significant number of changes occurring as the specification is developed. Real time protocol trigger and decode of the PD CC signal is required to be able to trigger on errors, and manage control packets or data packets during development.

USB 3.1 Transmitter (TX) and Receiver (RX)

In order to provide USB 3.1 product designers with information to understand channel loss considerations, the USB 3.1 specification provides a detailed table with loss profiles for all use cases. The acceptable loss budgets for each channel are key to ensuring interoperability of 5 Gbs and 10 Gbs USB speeds for hosts, devices and cables. Channel budgets are the basis of both TX and RX testing. In Figure 9, the table is grouped into three sections, the host, device, and the cable, including the interface connector types. This a reference for what channel models must be achieved by the design engineer for TX or RX calibration and/or test.



Data Rate	Host	Connector	Cable	Connector	Device
5G	10dB	Std A	7.5dB	Std B	2.5dB
5G	10dB	Std A	3.5dB	Micro B	6.5dB
5G	6.5dB	C	7dB	C	6.5dB
5G	10dB	Std A	3.5dB	C	6.5dB
5G	6.5dB	C	4dB	Std B	2.5dB
5G	6.5dB	C	4dB	Micro B	6.5dB
10G	8.5dB	Std A	6dB	Std B	8.5dB
10G	8.5dB	Std A	6dB	Micro B	8.5dB
10G	8.5dB	Std A	6dB	C	8.5dB
10G	8.5dB	C	6dB	Std B	8.5dB
10G	8.5dB	C	6dB	Micro B	8.5dB
10G	8.5dB	C	6dB	C	8.5dB

Figure 9. USB Gen 1 and Gen 2 loss budgets.

The Link Training Status State Machine (LTSSM) is a part of the USB architecture for maintaining reliable links, optimizing power consumption and providing an extremely fast and flawless data transfer rate. LTSSM manages the data rates of the USB link and uses various algorithms for the link's reliability and recovery from errors that may occur. At 5 Gbs the LFPS signaling, can used to setup the link. Now, with higher speeds of 10 Gbs, the LTSSM has become much more complex. LTSSM is the communication protocol that determines whether a link operates at Gen 1 speed (5 Gbs) or, if it can be negotiated up to Gen 2 speed (10Gbs). To achieve optimal data rates, it is important that the LTSSM functions correctly.

USB 3.1 Transmitter (TX)

In support of USB 3.1 TX test at up to 10G data rate, 14.5dB channel fixtures, with software integrated Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE), are needed to create the proper compliance channel. For pre-compliance test, a custom fixture can be used to break out the Type-C signals for analysis, embed the channel models, and also use the software integrated CTLE and DFE.

The USB 3.1 specification requires electrical tests that rely on proper setup and analysis for acceptable results. The spread spectrum clocking (SSC) modulation signal is a required test for USB 3.0 and 3.1 in regards to EMI and will ensure the device is able to transmit an accurate profile acceptable for receiver input. Also, the flippable USB Type-C cable requires the RX/TX process to be executed for both cable orientations. Setup and test execution, results analysis and debug can take many hours or even days to complete when done manually making automated test much more desirable.

USB 3.1 Receiver (RX)

SuperSpeed Capability Declaration (SCD) and LFPS Based Pulse Width Modulation Messaging (LBPM) are important components of USB 3.1 receiver testing. SCD is part of the link training status state machine (LTSSM) sequencing. Signal quality for these protocols and timing is very important. The DUT must generate the SCD1 and SCD2 signals while the signal quality measurements (period, rise and fall time, voltage, etc) are verified. These signals ensure the device is able to negotiate to the correct link (Gen1 or Gen2).

The USB 3.1 Rx calibration specification is quite complex with specifications for VPP, pre-shoot, de-emphasis, random jitter, sinusoidal jitter, eye height, eye width and more. Manual set up and test for these parameters is just not feasible, due to the many test variations that must be performed, and automated test is required.

USB Type-C cable/connection

Development and test of hosts and devices requires an understanding of the connected channel, especially regarding the standards tests that are performed. The USB Type-C channel including symmetrical connector, high-speed data, high power, multiple data transmission types, and backwards compatibility increase the number of configurations that need to be tested to verify USB channel conformance. Performance of the end-to-end link of the channel, in various configuration is affected by three signal integrity impairments: attenuation, reflection and crosstalk. Channel tests must also include removal of test fixture effect and manage additional effects on the channel response.

Keysight Solutions

Design and test engineers can save hours of work and have confidence in their test results when they use USB Type-C hardware, software and fixture solutions provided by Keysight Technologies. For the best results in Power Delivery, RX/TX and cable/connector test, the following tools and solutions supporting USB Type-C test are provided.

Power Delivery (PD)

N7016A Type-C low speed signal access and control fixture (Figure 10) manages power and control lines from the N7015A Type-C high speed test fixture to support termination requirements, test configuration, and connection to a power delivery controller. Easy access to CC1, CC2, Vbus and ground signals allows the breakout of USB 3.1 signals from USB devices for system diagnosis and control. The N7016A can simulate upstream or downstream devices and electronically flip the Type-C connection to thoroughly test PD functions.

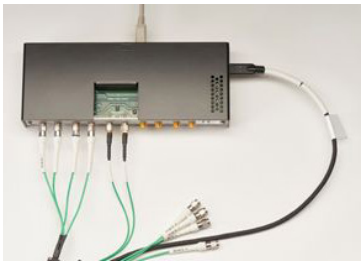


Figure 10. N7016A Type-C low speed signal test fixture.

Key features include:

- Access to CC1, CC2, SBU1, SBU2, VBUS and GND
- Controls to terminate CC1, CC2 independently (RA, RP, RD)
- Control to load VCONN
- External power for power consumers
- Type-C receptacle to connect with other devices or cables
- USB 2.0 interface for external control of application or standalone PC software

N8837A USB-PD Protocol Trigger and Decode software (Figure 11), for Infiniium Series oscilloscopes, provides a fast and easy way to debug the CC1/2, BMC encoded, 300 KHz signal with enhanced serial analysis capability for decode, listing window view, software searching and trigger.

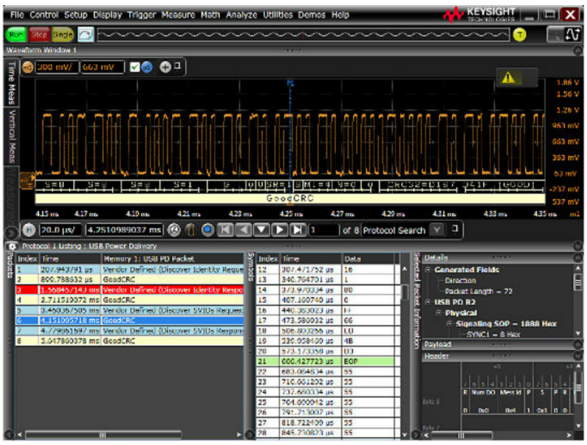


Figure 11. N8837A USB-PD protocol trigger and decode software for USB power delivery provides a fast and easy way to debug the Type-C CC1/2 signal.

Key features include:

- Support for the USB-PD CC 4b/5b BMC encoded protocol
- On-screen serial decode synchronized with serial waveform
- 4b, 5b or Label display formats
- Unique listing-window view of data transfer information with an automatic click and zoom and column sort
- Serial packet search with navigation controls
- Software trigger on search for orders Sets, Control Packets, Data Packets and Errors.

USB 3.1 Transmiter (TX)

The N7015A Type C test fixture (Figure 12) is for pre-compliance test and is designed for all the known Type-C standards and Alt modes, including 20G Thunderbolt 3, and features a breakout fixture with very short, low loss cables. The cables, including four pairs of RX/TX and the D+ and D- lanes, connect directly to an oscilloscope for the best signal integrity. De-embedding models for the N7015A are available and integrated into the compliance application and Infiniium oscilloscope baseline software. The SBU signals can also be viewed for Alt mode signals such as DisplayPort and Thunderbolt.

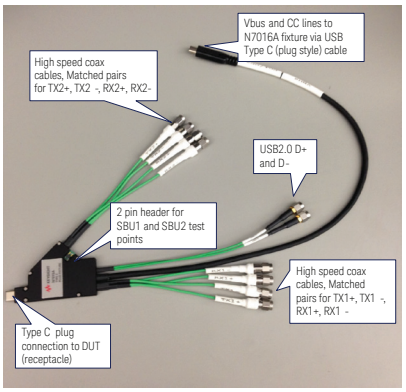


Figure 12. N7015A Type C test fixture.

N8821A USB 3.1 Gen1/Gen2 protocol trigger and decode software application (Figure 13), for Infiniium Series oscilloscopes, helps engineers to set up the oscilloscope to view USB 3.1 Gen1 (8b/10b) and Gen2 (128b/132b) protocol decode and quickly troubleshoot any protocol issues. It includes a suite of configurable USB 3.1 protocol-level searches and software-based triggering. A viewer enables correlation between waveforms and selected packets allowing the user to quickly move between the physical and protocol layer information using a time-correlated tracking marker.

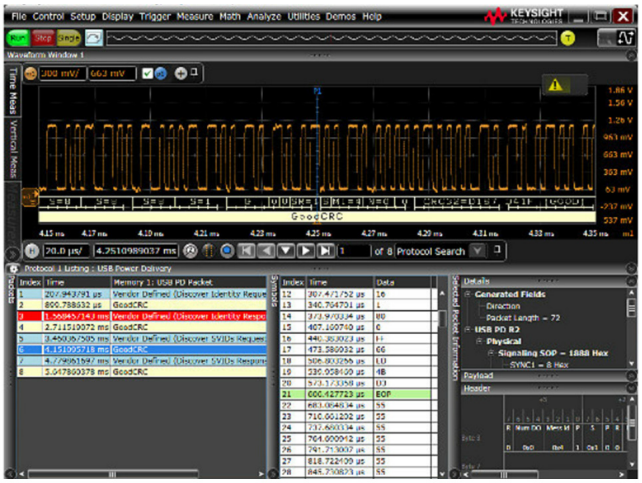


Figure 13. N8821A USB 3.1 Gen1/Gen2 protocol trigger and decode application includes a suite of configurable protocol-level searches and sofware-based triggering specific to USB 3.1.

U7243B USB 3.1 compliance test software (Figure 14), for Infiniium oscilloscopes, provides engineers with automatic execution of USB 3.1 electrical tests, including setup and results analysis with comparison to published specification limits. Robust debug tools are available to help with root-cause analysis of issues.

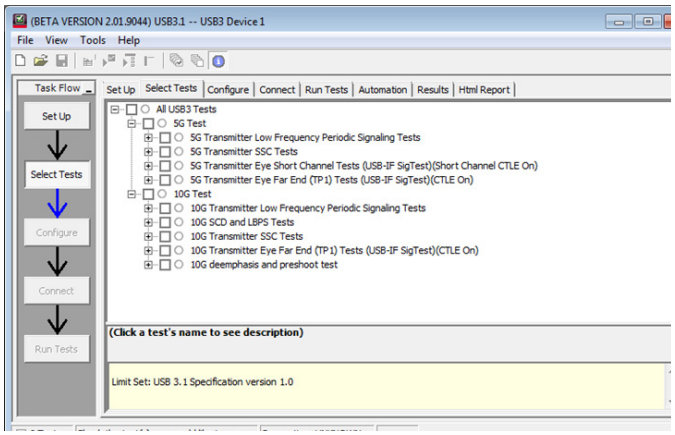


Figure 14. U7243B USB 3.1 compliance test software provides a way to validate and debug USB 3.1 silicon, host, hub or device.

USB 3.1 Receiver (RX)

The N5990A Automated compliance and device characterization RX software (Figure 15) is a multi-bus stimulus/response test software for the USB 3.1 digital high-speed interface bus. The USB link training suite is a sequence generation tool for USB 3.1 Gen1/2 and provides control for SCD1/SCD2/LBPM cycles, TSEQ count, TS1 and TS2 count. LFPS tPeriod, tBurst, tRepeat, tPWM and other parameters can easily be adjusted. Engineers also have a choice of a power on sequence or a warm reset sequence for test.

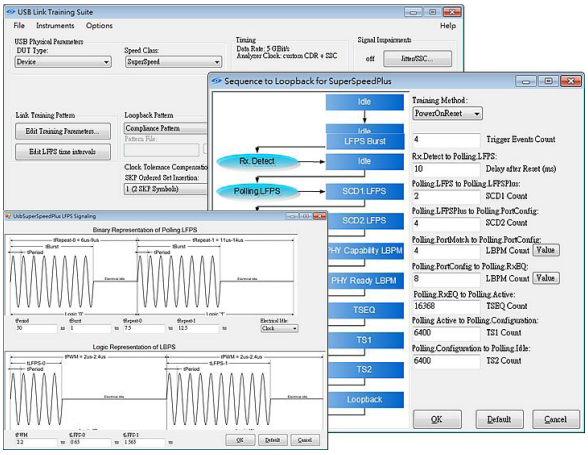


Figure 15. N5990A test automation software platform for testing a wide range of digital buses including USB.

M8020A Receiver test setup

The M8020A J-BERT high performance BERT (Figure 16) enables fast, accurate receiver characterization of single and multi-lane devices running up to 16 or 32 Gb/s and had been specifically designed to help with USB 3.1 Gen 2 testing. Generation of calibrated RX test stress conditions such as SSC, sinusoidal jitter (SJ), random jitter (RJ),
de-emphasis, and ISI are possible. It provides support for 8b/10b and 128v/132b coding and as well as scrambling. It has integrated link training hardware and software built in along with Tx Eq, noise impairment, variable ISI, and receiver equalizer/eye opener.

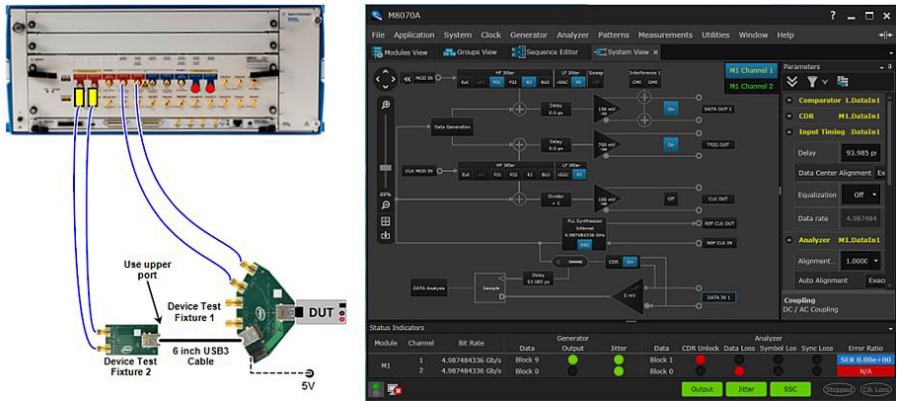


Figure 16. M8020A J-BERT enables receiver characterization of single- and multi-lane devices.

USB Type-C cable/connection

The USB Type-C cable/connector compliance test consists of an ENA mainframe (E5071C) with the enhanced time domain analysis option (E5071C-TDR) and an N4433A ECal module with automated USB cable and connector test software. Fixtures for testing USB Type-C connectors and cables may also be needed. The Luxshare-ICT test fixtures can be found at http://web.luxshare-ict.com/en/. Keysight documentation for “Method of Implementation” (MOI) including instrument setup files is available for free download and Keysight.com.

Summary

Keysight experts work closely with the USB Type-C standards and are intimately familiar with the changes and new capabilities, as well as, the increased complexity of test. Engineers faced with the new challenges of USB Type-C test in Power Delivery, RX/TX and cable/connector can benefit by choosing the solutions provided by Keysight. Regardless of which USB generation or USB Type-C design and test challenges you are facing, Keysight offers a complete solution set from simulation to compliance. Gain insights faster with Keysight test solutions, proven test systems for specific applications. Developed to solve critical test issues for specific applications, the test solutions provide the hardware, software and fixtures for the technical foundation of your test system.

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