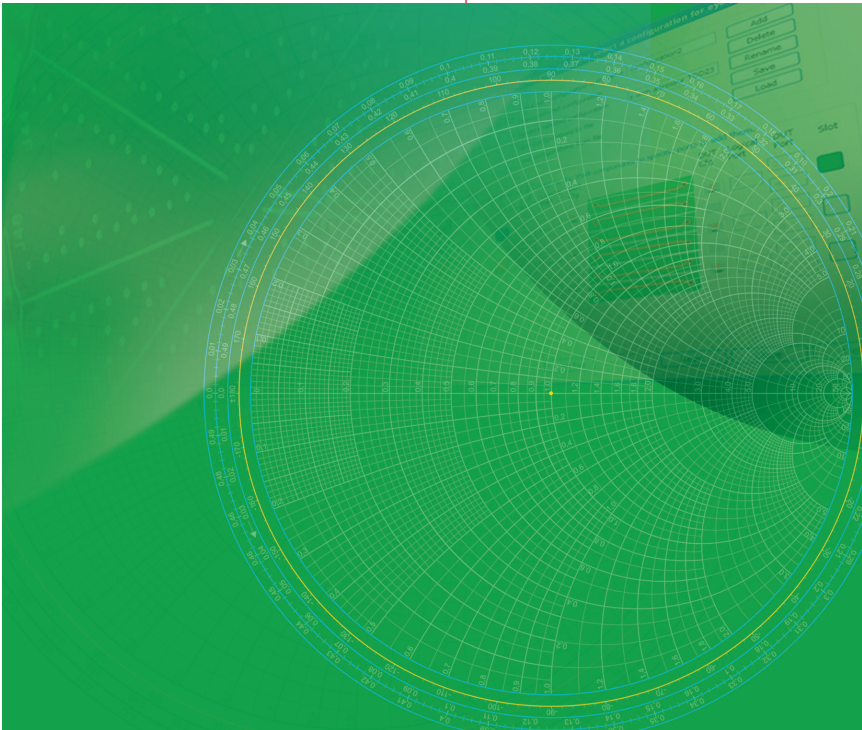


# Keysight Technologies

## Using the Time-Domain Reflectometer

Application Note  
S-Parameter Series



## Analysis of High-Speed Digital Interconnect: Measuring S-parameters

*Today's Time Domain Reflectometers provide digital design engineers with powerful tools that not only display traditional impedance measurements, but they also provide ease-of-use that generate S-parameter measurements that may be used for de-embedding purposes.*

As data rates for digital designs increase into the multi-gigabit per second (Gbps) range, frequency dependent effects become a more prominent challenge than in the past. The proliferations of today's high-speed serial digital standards demand differential circuit topology and a more rigorous measurement and simulation analysis is required to achieve the design goals of the advanced differential physical layer. It is now necessary to consider both time and frequency domain analysis to achieve proper characterization.

For decades now, RF and microwave engineers have used a vector network analyzer (VNA) to analyze their high-frequency designs. The VNA performs measurements natively in the frequency domain and yields S-parameters directly.

Digital designers, on the other hand, are often more familiar with time domain measurements performed using an oscilloscope equipped with time-domain reflectometry (TDR) capability. TDR natively displays signal reflections versus time (or position) of the discontinuity; that is, the impedance profile of the circuit is derived directly from the reflected signal. As a result a TDR instrument is often more intuitive for digital engineers to use, but new multi-gigabit designs require that they must also become more familiar with the properties of microwave signals. While this more complex analysis often requires use of both a VNA and TDR, this paper will focus on use of a TDR instrument in generating S-parameters that may be used for embedding/de-embedding purposes.

### The Keysight TDR System

It's important to select the right tool for the job. The Keysight 86100D DCA-X Wide-Bandwidth oscilloscope equipped with 54754A Differential and Single-ended TDR/TDT module(s) provides the necessary bandwidth and edge speed to accurately characterize designs to 10 Gbps and beyond. The built-in calibration routine removes cable losses and also allows users to increase the TDR edge speed from 35 ps (raw hardware performance) to an effective TDR edge speed of < 20 ps. If S-parameter measurements to 50 GHz are required using a TDR system, the 54754A TDR/TDT module may be coupled with Picosecond Pulse Labs 4022 (PSPL) source enhancement module and the Keysight 86118A Dual 70+ GHz remote head receiver module. This high-precision combination enhances the resolution even further and provides sub-millimeter two-event resolution using a nine-picosecond TDR step.

## A brief overview

Time domain reflectometry is a common method for verifying and analyzing transmission line properties of a variety of components and circuits such as printed circuit board (PCB) traces, vias, cables and connectors. The TDR instrument sends a pulse through the medium and compares the reflections from the unknown transmission environment to those of the incident pulse. It then calculates and displays impedance versus time/distance for the device under test. Its complement, Time Domain Transmission (TDT) measures the step after it passes through a device and can be used to determine other relative transmission parameters such as step response, rise time/pulse degradation, as well as propagation times and dielectric loss attenuation.

By performing a Fast-Fourier Transform (FFT) on the measured time domain data, frequency domain information can be readily attained. Return loss, insertion loss, near-end and far-end crosstalk are a few of the common frequency domain measurements that can be calculated by performing an FFT on the measured TDR/TDT data. 86100D-202 Enhanced Impedance and S-parameter software allows users to perform calibrated, real-time measurements on the 86100D DCA-X mainframe without the use of external software. If more advanced analysis is required, the N1930B Physical Layer Test System (PLTS) software is PC-based software that can control the 86100D system and provide advanced signal integrity capabilities including standards-based compliance measurements.

## A bit of math

The digital designer has to be comfortable with the S-parameter technique of modeling a device under test (DUT). A quick look at the formulas that determine time or frequency measurements shows a remarkable similarity. For the time domain:

$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{load} - Z_0}{Z_{load} + Z_0} \quad Z_{DUT} = Z_0 * \frac{1 + \rho}{1 - \rho}$$

For the frequency domain:

$$S_{11} = \frac{V_{reflected1}}{V_{incident1}} = \frac{Z_{input(DUT)} - Z_0}{Z_{input(DUT)} + Z_0} \quad Z_{input(DUT)} = Z_0 * \frac{1 + S_{11}}{1 - S_{11}}$$

A closer look reveals that the equations are related via Fourier Transform. Time domain and transmission data can be obtained from frequency S-parameters, and vice-versa, using fast Fourier Transforms with boundary and windowing techniques. The data can then be fed to software platforms such as Keysight's PLTS, which can work and convert in either domain, for detailed analysis. While this is a simplified interpretation of the process, a detailed discussion of time/frequency conversion techniques is available from any number of sources that the reader may peruse at their discretion. But the point is that the digital designer can continue to work within the TDR comfort zone, but easily obtain results equivalent to those in the frequency domain.

## TDR versus VNA

Paper two discussed the collection of S-parameter data for high-speed interconnect using a VNA. VNAs employ a tunable narrowband receiver and a swept sine wave stimulus to perform their frequency based measurements. Since the noise floor of a test system is proportional to the square root of the bandwidth of the receiver, the narrowband VNA therefore has a much lower noise floor and higher dynamic range than a TDR based measurement. VNAs also offer more advanced error correction techniques (Automatic Fixture Removal, Differential crosstalk calibration and TRL Wizard) along with higher port count (up to 24 ports) and faster risetimes (110GHz = 6.5 picosecond) than a TDR system.

TDR instruments, on the other hand, use a wide-bandwidth receiver and use a fast step as the stimulus. They are capable of measuring much lower in frequency than a typical VNA (near DC using TDR versus 10 MHz on a VNA unless more advanced measurement techniques are utilized) which is one reason why many signal integrity engineers utilize both TDR and VNA based measurements in their labs. As mentioned before, many digital designers find TDR systems more intuitive to use than VNAs. Finally, since most TDR systems are based on an oscilloscope platform, the equipment can also be used to perform waveform measurements and analysis.

The TDR can directly provide a variety of measurements including:

- First order topology models
- S-parameter models (with the use of PLTS or TDR option firmware)
- Characterize rise time degradation
- Interconnect bandwidth
- Near and far end cross talk
- Odd/even mode, differential/common impedance
- Mode conversion
- Complete differential channel characterization

## The device under test (DUT)

The performance of high-speed semiconductors is usually validated using custom-designed fixtures. Signals are usually routed from the balls (or pads) of an integrated circuit (IC) to coaxial connectors through differential traces on the test fixture. Cables are then used to connect the signal from the connectors to an oscilloscope for waveform characterization. While this connectorized setup provides more accurate and repeatable measurements than could be realized by probing, the fixture and cable still degrade the signal.

In order to maximize margins and/or provide better part specifications, designers often want to de-embed the effects of the fixture and any cables. De-embedding software requires accurate S-parameter models - without accurate models, de-embedding software will yield disappointing and inaccurate results.

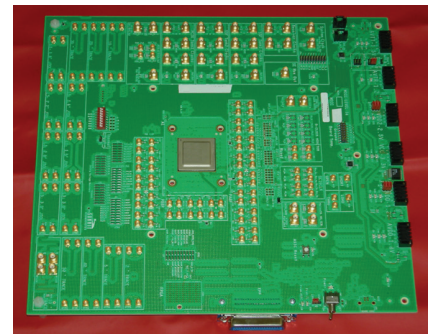


Figure 1. A typical test fixture used to characterize new semiconductor designs

## Obtaining S-parameters of a fixture to use for de-embedding

Below are the recommended steps to generate useful S-parameter models using a TDR-system:

1. Perform time-domain (impedance) measurements. Analyze the results.
2. Convert to frequency-domain. Analyze the results.
3. Examine and correlate characteristics seen in (1) and (2).
4. Generate the S-parameter file.
5. Validate the model using simulations and measurements.

This paper documents the steps used to analyze a differential trace on a demo board (test fixture) designed to support data rates up to 5 Gbps. It details S-parameter file generation intended for de-embedding and analyzes a de-embedded signal using the 86100D-SIM Waveform Transformation Toolset.

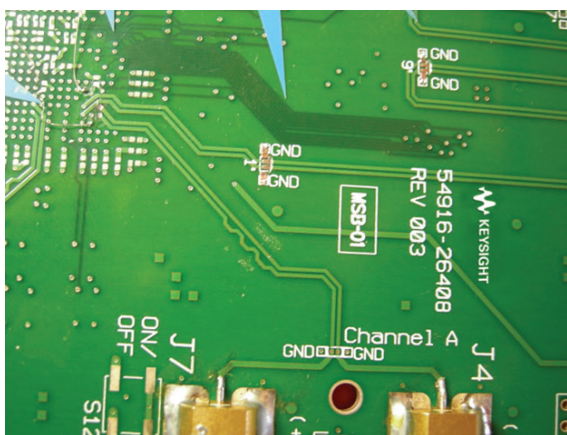


Figure 2. Device Under Test (DUT) - "Channel A" is a differential trace connecting the BGA of an FPGA (upper left) to connector J4 and J7 (bottom center).

## Obtaining S-parameters of a fixture to use for de-embedding

### 1. Perform time-domain measurements. Analyze the results.

The Keysight TDR system is setup for Differential stimulus into the J4/J7 connectors of the device under test (DUT). Prior to making measurements the system should be de-skewed using PLTS or the built-in de-skew routine. During this initial time-domain investigation TDR/TDT calibration is optional.

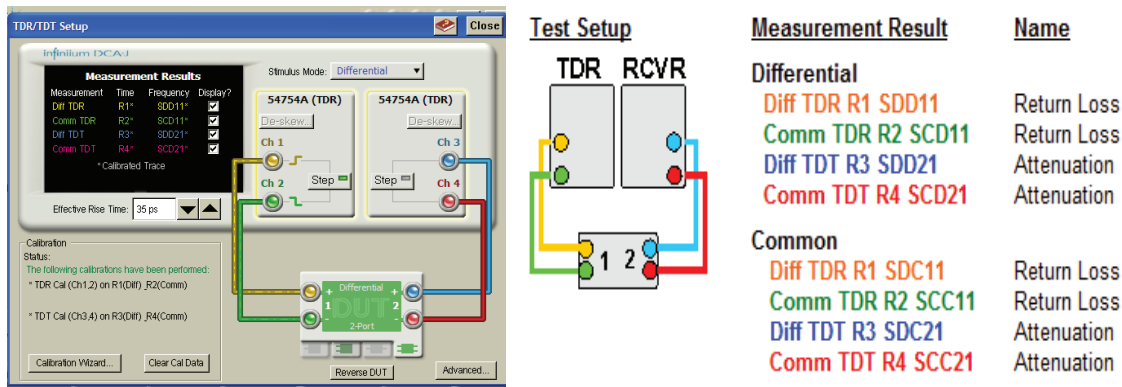


Figure 3. The 86100D DCA-X provides a graphical user interface which makes it easy to setup the TDR/TDT measurement (Port 1 = DUT J4/J7 connectors; Port 2 = DUT BGA)

We begin the analysis by looking at the Differential response to a Differential stimulus, SDD11, or trace R1.

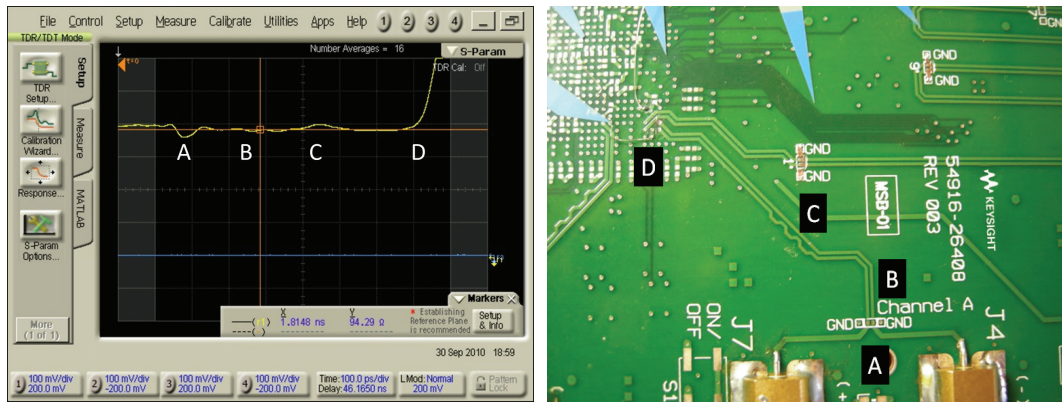


Figure 4. Trace R1 (yellow) shows a TDR measurement looking into the differential trace from connectors J4/J7 (point A).

### Identifier description

- A. Discontinuity at connector launch (J4/J7)
- B. Differential impedance is ~ 95 ohms after the connectors
- C. Unknown discontinuity
- D. Open at BGA (unloaded board)



## Obtaining S-parameters of a fixture to use for de-embedding

### 1. Perform time-domain measurements. Analyze the results *(continued)*

To better understand what could be causing the discontinuity at point C, we can look at the Common Mode response. The Common response to a Differential stimulus shows imbalances in the design that can cause mode conversion. With the TDR stimulus still set to Differential, the Common response, R2 (green trace), is displayed in Figure 5.

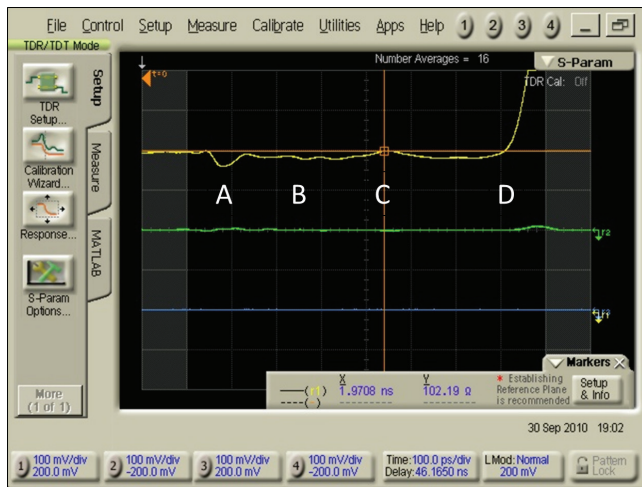


Figure 5. Common response (R2, green trace) to a Differential stimulus. Little to no mode conversion is evident at point C.

As seen by the relatively flat response in R2 (green trace) at point C, no mode conversion is taking place. What else could be going on to cause the anomaly at point C? Let's have a look at each side of the differential trace (D+ and D-) separately, that is, look at them as single-ended traces.

We can compare them most easily if we invert one of them using a math function. Math 3 (blue) inverts the D- trace while Math 4 (red) displays the D+ trace.

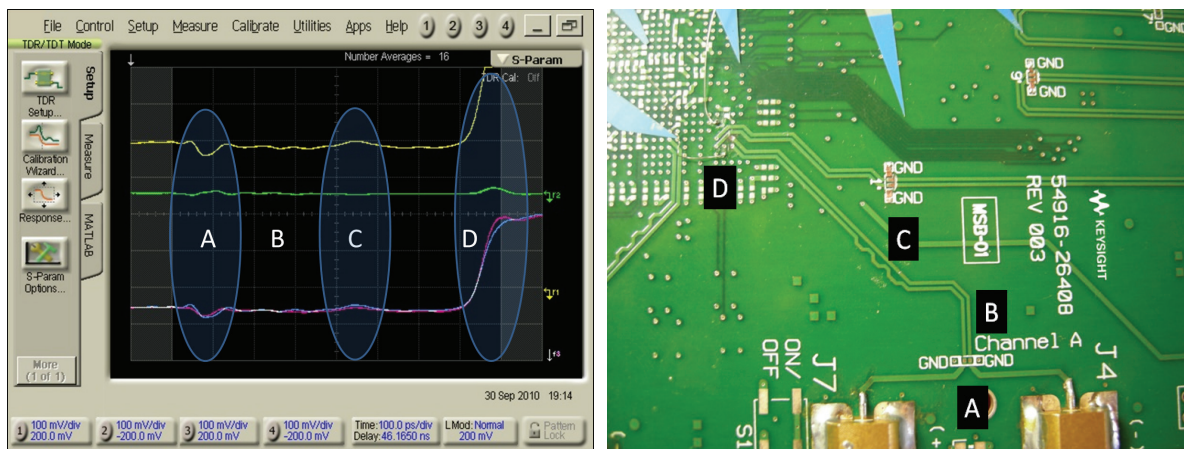


Figure 6. Impedance measurements of each leg of the differential trace, D+ (red) and D- (blue).

Region A in Figure 6 is the location where the differential trace is split and the signals are routed to the SMA connectors on the edge of the board. Although one can see small differences in the impedances this will not cause mode conversion since the propagation is uncoupled in this region. The differences in the impedance may simply be due to soldering.

## Obtaining S-parameters of a fixture to use for de-embedding

### 1. Perform time-domain measurements. Analyze the results *(continued)*

It's possible to see why Region B exhibits excellent differential impedance performance. The differential lines are routed next to one another with no other traces nearby.

Both D+ and D- show a similar impedance variation in Region C which is an indication that there is an issue influencing both traces in this area. By looking at the traces on the board it appears as though some purposeful mismatch was introduced, or perhaps this zigzag pattern was added so as to match trace lengths (minimize skew). In any event it induces little imbalance, but it does change the differential impedance significantly.

As seen in Region D, the impedance characteristics of D+ and D- are different in area of the Ball Grid Array (BGA) field. There must be some type of imbalance in the BGA vias, and since the traces are coupled in this region, mode conversion will likely occur. Let's have a look at the physical structure on the board to see what is going on.

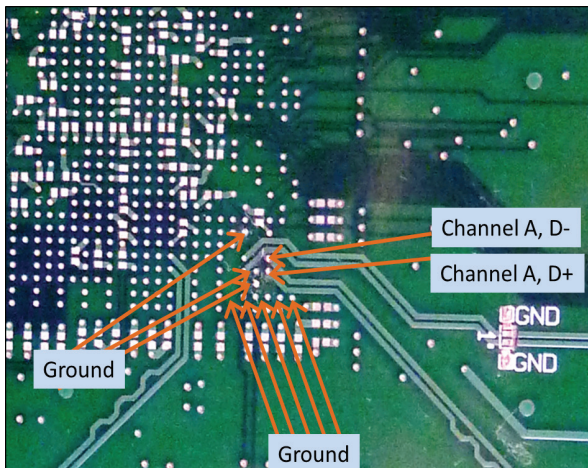


Figure 7. Fewer grounds in the BGA near D- compared to D+ causes an impedance imbalance.

Using the Keysight N1021B 18 GHz Differential Probe, it is also possible to perform a TDT measurement and examine the Step Response of the differential pair. Using a differential stimulus, the 86100D displays the differential TDR (R1, yellow trace) and differential TDT (R3, blue trace) in Figure 8. Notice that there is a fairly significant re-reflection at point 2. Also notice that the shape of the reflection at point 2 is similar in structure (same polarity, relative size of peaks) to the original step (point 1).



## Obtaining S-parameters of a fixture to use for de-embedding

### 1. Perform time-domain measurements. Analyze the results (continued)

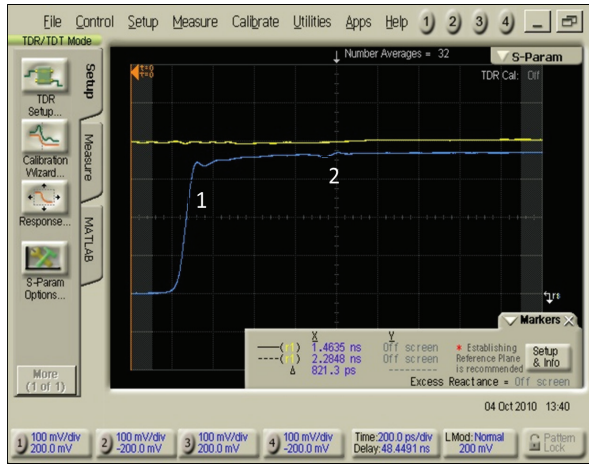


Figure 8. Differential TDT (blue trace) showing the Step Response of the differential pair. Point 2 is caused by a re-reflection.

We've learned a great deal about this differential trace by using the Keysight TDR equipment to perform TDR and TDT measurements. There is also a great deal of insight that can be learned by analyzing the design in the frequency domain.

### 2. Convert to frequency-domain. Analyze the results.

86100D-202 Enhanced Impedance and S-parameter software makes it easy to perform S-parameter measurements in real-time. Alternatively, Keysight N1930B PLTS also controls the 86100D and allows users to display multiple S-parameter measurements at the same time.

By pressing the S-parameter tab in 86100D-202, a shade drops down to display the S-parameter data. Figure 9 displays the differential return loss (SDD11) and differential insertion loss (SDD21) for Channel A of the fixture. The return loss is ~ 10 dB while the 3 dB bandwidth of this channel is less than 4 GHz.



Figure 9. Return loss (SDD11) and insertion loss (SDD21) for Channel A as measured by 86100D Option 202 Enhanced Impedance and S-parameter software.

## Obtaining S-parameters of a fixture to use for de-embedding

### 2. Convert to frequency-domain. Analyze the results (*continued*)

Since the fixture is made of FR4 material, we'd expect a gradual roll-off with increasing frequency. What we see, however, is a null of almost 50 dB at approximately 14.5 GHz. Often a null such as this indicates a reflection(s) due to two discontinuities in the circuit. Spacing between the discontinuities is given by:

$$S_{11} = \frac{V_{\text{incident}} - Z_{\text{equivalent}} \cdot I_{\text{incident}}}{V_{\text{incident}} + Z_{\text{equivalent}} \cdot I_{\text{incident}}} = \frac{1 - S_{11}}{1 + S_{11}}$$

Where:

- C = speed of light = 3E8 m/s
- E<sub>r</sub> = FR4 dielectric = 4.2 ~ 4.5
- Frequency = 14.5 GHz

Spacing between the discontinuities is ~ 10 mm. So what could be causing this null in the frequency domain?

### 3. Examine and correlate any characteristics seen in (1) and (2).

Let's go back to our fixture and look for physical structures that are spaced by 10 mm. As shown in Figure 10, it turns out that there are several structures that are about 10 mm in length. This is likely root cause for the deep null at ~ 14.5 GHz. This null will introduce significant inter-symbol interference (ISI) and limit the data rate that this board design will support. It will also degrade the quality of the file for de-embedding purposes.

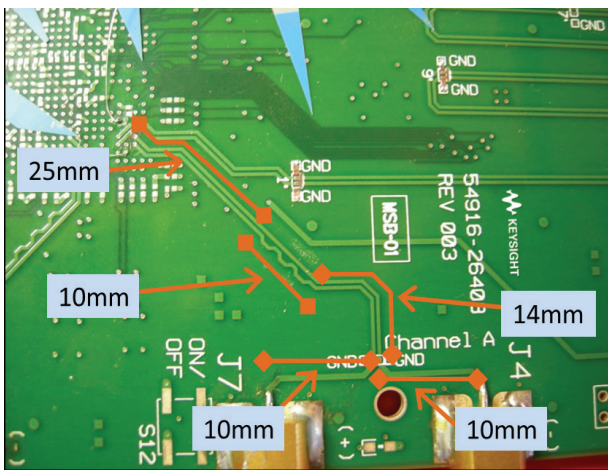


Figure 10. Physical measurements of different sections of Channel A reveal several structures having lengths of ~10 mm.

The frequency domain view suggests that this design will support data rates of several Gbps. The fundamental frequency of a 5 Gbps signal is 2.5 GHz, therefore the insertion loss (attenuation) of the 3rd harmonic (7.5 GHz) is ~ 8 dB. However, if the data rate was increased to 10 Gbps, for example, the null at ~ 14.5 GHz would cause severe signal integrity issues. The 50 dB null at ~15 GHz will greatly attenuate the 3rd harmonic (3\* 5 GHz = 15 GHz) and the eye quality will suffer. Further, if a designer wanted to de-embed this fixture, the high loss at 15 GHz would introduce a tremendous amount of ringing due to the amount of gain required at 15 GHz.

## Obtaining S-parameters of a fixture to use for de-embedding

### 4. Generate the S-parameter file

There are several best practices to follow when measuring S-parameters using a TDR. They include:

- a. Use high quality calibration standards to remove cable/probe effects.
- b. Use short, high quality cables.
- c. De-skew cables.
- d. Use averaging during TDR/TDT calibration (e.g. 256) and while making measurements (e.g. 64); averaging lowers the measurement noise floor.
- e. If probing:
  - i. Use a probe pin configuration that includes adjacent grounds (e.g. GSSG). The availability of grounds is made possible by good planning during layout. Note – For devices that are linear and time invariant (e.g. traces on printed circuit boards, connectors, cables, etc.), differential S-parameters can be calculated from single-ended probe (e.g. GSG) measurements.
  - ii. Use a probe station/holder to yield accurate, repeatable results. While browser style probes are convenient for troubleshooting DUTs, they are not recommended for generating S-parameter files to be used for de-embedding (no adjacent grounds).
- f. Ensure adequate frequency point spacing in the S-parameter file. To ensure amplitude and phase content is accurately represented in the file, and to ensure it captures the effects of re-reflections, the following setup parameters are recommended:

Recommended Frequency Spacing =  $1 / (20 \times \text{DUT length})$ .

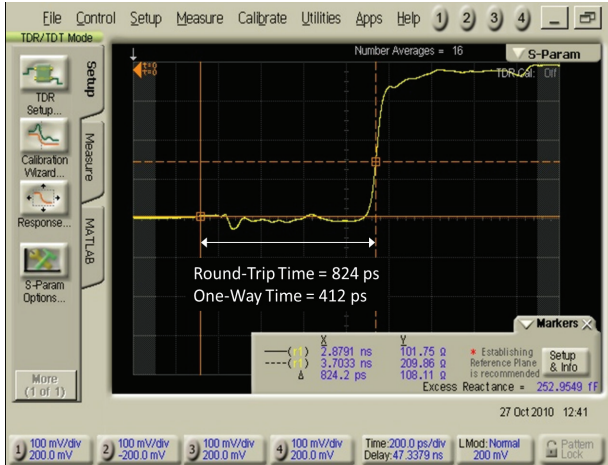


Figure 11. TDR measurement using markers to determine the electrical length of the DUT.

As shown in Figure 11, the electrical length of this DUT is ~ 412 ps. To achieve the desired frequency spacing of 100 MHz:

- Full Screen Time Range =  $1/\text{Frequency Spacing} = 1/100 \text{ MHz} = 10 \text{ ns}$
- Time per Division = Full Screen Time Range/10 divisions =  $10 \text{ ns}/10 \text{ div} = 1 \text{ ns/div}$

## Obtaining S-parameters of a fixture to use for de-embedding

### 4. Generate the S-parameter file continued

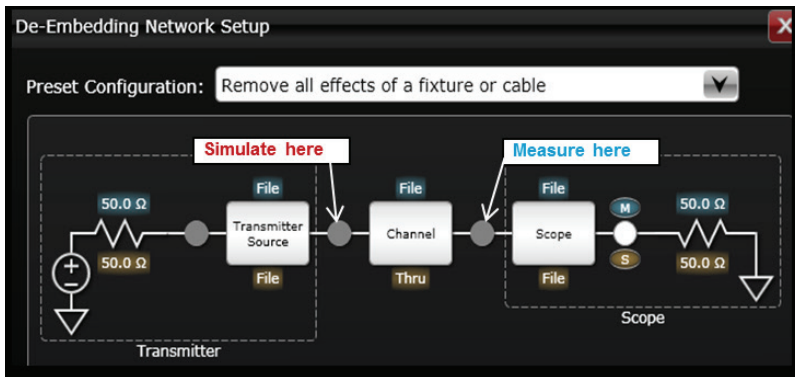
To capture S-parameters to 20 GHz:

- Frequency Range = # Points / Time Range. However, taking into account Nyquist, the “usable” frequency range is given by:
- Usable Frequency Range = # Points / (2xTime Range)  
Rearranging the formula allows us to determine how many points per waveform we should use.
- # of Points = 2xTime Range \* Usable Frequency Range
- # of Points = 2(10 ns)(20 GHz) = 400 points
- The DCA has a minimum of 512 points per waveform in TDR mode.

With the S-parameter data displayed on the DCA using Option 202, the data may be saved directly into a Touchstone file format (\*.s4p). Alternatively N1930B PLTS software makes it easy to import the trace data and generate Touchstone files as well.

### 5. Validate the model using simulations and measurements.

There are several software packages on the market today that allow engineers to simulate signals using their S-parameter models. Keysight ADS, PLTS and FlexDCA are a few of them. N1010A FlexDCA is integrated into the 86100D’s user interface and when equipped with Option SIM, offers true embedding/de-embedding software capabilities. A graphical signal processing interface makes it easy to setup the measurement.



#### Simulate waveform using model

(input → apply S-parameter model → output)

- simulate expected DUT TX signal (e.g. 10Gb/s, PRBS7, Rise/Fall Time = 25ps)

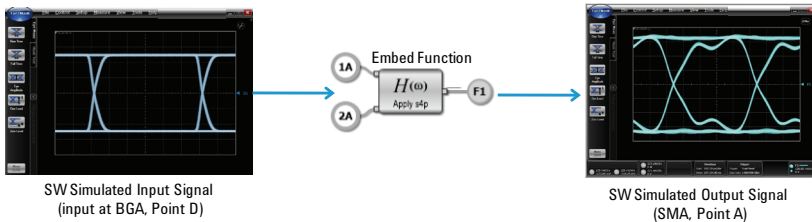


Figure 13. Predict the output waveform using simulation software such as FlexDCA.

## Obtaining S-parameters of a fixture to use for de-embedding

### 5. Validate the model using simulations and measurements *(continued)*

#### Verify model and waveform with an actual measurement

(inject signal from PG → actual DUT → measure output)

- generate expected DUT TX signal using BERT, inject via probe, measure on scope

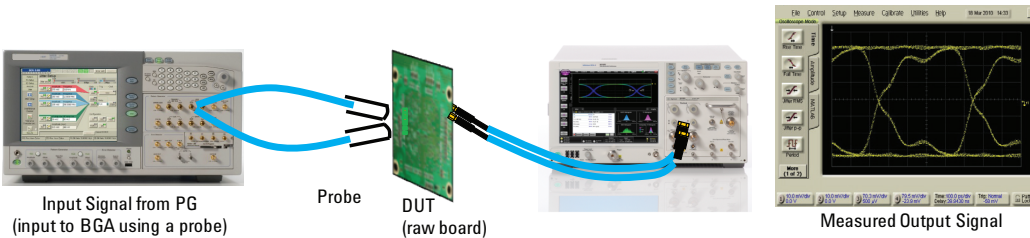


Figure 14. Validate your S-parameter model by comparing the simulation with an actual measurement.

By comparing the output waveforms as shown in Figure 13 and 14, there is excellent correlation between simulated and measured waveforms. This gives the designer confidence that the S-parameter model is accurate and may be used for simulation and de-embedding purposes.

Waveform Analysis Tip: If the eye diagram of the de-embedded signal appears noisy, switch into Oscilloscope mode and look for ringing on the single-valued waveform (bit sequence). Use markers to look at the period and/or frequency of the ringing. Often this ringing is caused when attempting to de-embed using a model with excessive loss. For example, if the model has 20 dB loss at 14 GHz, the de-embed function will apply ~20 dB of gain. Any energy in the signal at that frequency (data rate dependent), along with noise, will be amplified by the de-embed function. This illustrates why many designers try to limit the gain applied by de-embed functions to less than 10 dB.

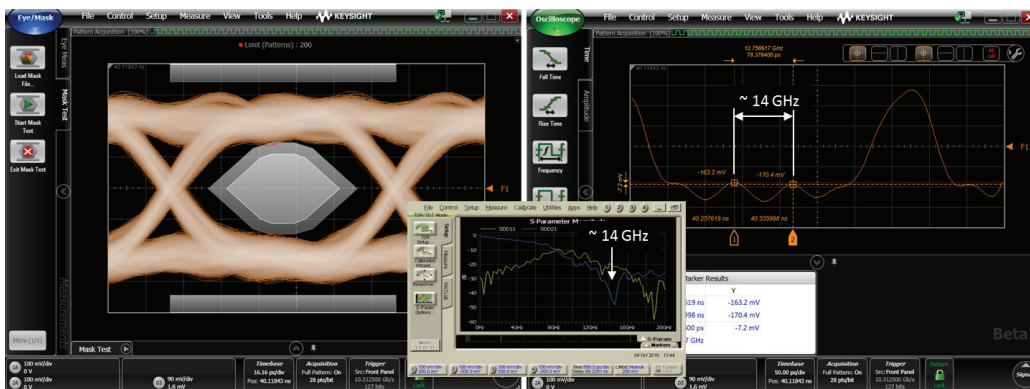


Figure 15. The de-embedded signal (left) appears noisy; when the bit sequence is analyzed in Oscilloscope mode, ringing is observed at the same frequency (~ 14 GHz) as a significant null in the SDD21 response.

It is also a good practice to setup the de-embed function such that the software filter will roll-off at a null in the incoming data signal (e.g. 4th or 6th harmonic) since this will also help to minimize ringing in the de-embedded waveform.



## Conclusion

This third paper in the series detailed the use of a TDR system to gain powerful insight into impedance discontinuities of a digital design, and covered best practices to use when generating S-parameter files for de-embedding purposes. The paper also provided methods to validate models using Keysight 86100D DCA-X based simulations and measurements. N1930B PLTS is a powerful signal integrity tool that allows today's high-speed digital designers to control both VNA and TDR based instruments. Many high-speed signal integrity labs employ both TDR and VNA systems to leverage the benefits of both instruments.

The next paper in this series will discuss how to determine S-parameters using an EM model and Keysight's ADS.



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