

# Keysight Technologies

## Optimize Power Source Integrity Under Large Load Transients

### What's Inside:

- Why voltage drops occurs
- How to achieve the lowest possible voltage drop by:
  - Building optimal load leads
  - Selecting the right power supply
  - Using local bypassing

### Application Note





## Introduction

Today's integrated circuits are operating faster than ever. The increased operating speed can lead to highly dynamic power demand from the power supply, which poses a challenge during testing when you source power using programmable power supplies. The high-speed current waveforms can lead to voltage drops at the integrated circuit. If it is severe enough, the voltage drop can reset the microprocessor or cause anomalies in your test results. This application note explains why this voltage drop occurs and offers several ways to achieve the lowest possible voltage drop by selecting optimal load leads and power supplies and using local bypassing.

## Selecting Programmable Power Supplies

Traditionally, to achieve the best possible output voltage regulation, you would use a linear power supply. However, at higher current levels, linear power supplies tend to be very large, expensive and highly inefficient. Recent advances in switching power supply technology make it possible to replace linear power supplies with switching power supplies in performance applications.

Switching power supply designers are faced with seemingly contradictory goals of low output noise, fast transient response, low cost and high density. Achieving low output noise is usually achieved with multiple stages of filtering or using larger filter components, both of which lead to higher cost, lower power density and slower transient response. More advanced power supplies employ higher switching frequency, better filter design and more sophisticated control topologies to optimize all of the criteria. When you select a power supply for IC test applications, it is important to examine the voltage transient response specification and output impedance characteristics to ensure good performance.

## Optimizing Load Wiring

In many cases, physical constraints force you to position the power supply several feet away from your IC test board, necessitating at least a few feet of load lead wiring. Load lead wiring impedance can very quickly degrade the source impedance experienced by the IC. Almost all programmable power supplies provide sense lead inputs, which allow you to select the point of voltage regulation by connecting the voltage sense leads at that location. In this application, the sense point would be as close as possible to the IC. However, the voltage regulation loop can suppress voltage transients at this sense point only within its control bandwidth. Consequently, a voltage transient can occur at this sense point as long as the current transient rise time is sufficiently fast. Load lead impedance at these lower frequencies can be modeled as a lumped series inductance and resistance, as shown in Figure 1.

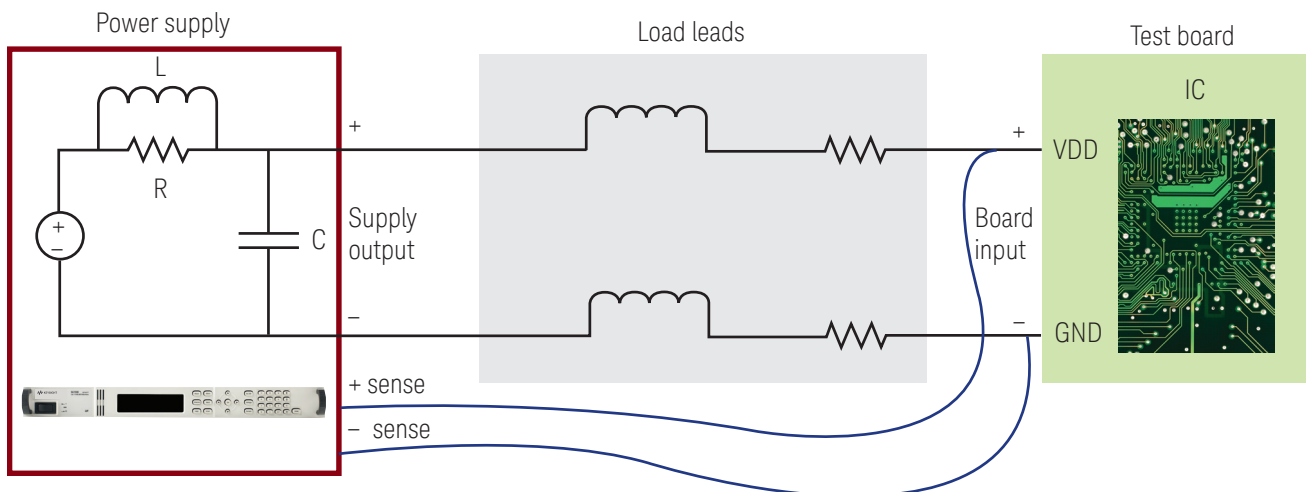


Figure 1. Simplified power supply output impedance and load lead impedance

Let's examine a 25-amp application with 5-amp transients where the power supply is set to 2.5 V and connected to the IC test board via 5 feet of 14 AWG wiring. Since this is a low-voltage application, voltage undershoots greater than 100 mV are generally not acceptable. 14 AWG wiring has 2.5 milliohms of resistance per foot, resulting in 25 milliohms of resistance for the round trip connection between the output of the power supply and the IC test board.

$$\begin{aligned} V_{(\text{drop-R})} &= R_{\text{lead}} \times I_{\text{tran}} \\ \text{Eq. 1} \quad V_{(\text{drop-R})} &= 0.025 \, \Omega \times 5 \, \text{amps} = 125 \, \text{mV} \end{aligned}$$

The calculated 125 mV of drop will be compensated by the power supply voltage control loop in a manner commensurate with its bandwidth. However, in the meantime, the IC will experience this 125 mV of voltage drop. In this application, the effect of the load lead resistance alone is enough to cause an unacceptable short-duration drop at the test board. However, the load lead inductance is another major factor that needs to be examined. It is not uncommon for the test board to ramp the 5-amp transient in a matter of 10 microseconds. This high rate of current change can cause a constant voltage drop across the leads during the current ramp. To characterize this voltage drop, it is necessary to make an approximation, since the exact load lead inductance can vary based on the proximity of the positive and negative load leads. In most cases non-twisted load wiring can be modeled as a 250-nH/ft inductor.

$$\begin{aligned} V_{(\text{drop-L})} &= L \frac{I_{\text{tran}}}{t} \\ \text{Eq. 2} \quad V_{(\text{drop-L})} &= 2 \times 5 \, \text{ft} \times 250 \times 10^{-9} \, \text{H} \times \frac{5}{10 \times 10^{-6} \, \text{sec}} \\ V_{(\text{drop-L})} &= 1.25 \, \text{V} \end{aligned}$$

Combining the effect of the resistance and inductance leads to:

$$\begin{aligned} V_{(\text{drop-total})} &= V_{\text{drop-R}} + V_{(\text{drop-L})} \\ \text{Eq. 3} \quad V_{(\text{drop-total})} &= 125 \, \text{mV} + 1.25 \, \text{V} = 1.375 \, \text{V} \end{aligned}$$

Clearly, the final result of 1.375 V is not acceptable. As mentioned previously, the power supply's voltage regulation loop will sense this voltage transient and will adjust the output of the supply by the necessary amount to maintain a steady 2.5 V at the test board. However, this process can take up to a millisecond, even with a good-performance power supply. The lead inductance effect can be mitigated by tightly coupling the force leads together, by either tying them together tightly at regular intervals or simply twisting them together. Twisting the leads also provides the added benefit of better immunity to other magnetic fields that may be present due to other load leads carrying large current transients. Twisted leads can be modeled as a 170-nH/ft inductor. This inductor includes both the positive and negative lead inductance effects. Recalculation with twisted leads yields:

$$\begin{aligned} V_{(\text{drop-L}_{\text{twisted}})} &= 5 \, \text{ft} \times 170 \times 10^{-9} \, \text{H} \times \frac{5}{10 \times 10^{-6} \, \text{sec}} \\ \text{Eq. 4} \quad V_{(\text{drop-L}_{\text{twisted}})} &= 0.425 \, \text{V} \end{aligned}$$

Although the voltage drop has improved, the total result is not yet acceptable. Further improvement can be made by paralleling cable runs. For example, paralleling four sets of twisted cables will reduce the resistance and inductance by a factor of four.

$$\text{Eq. 5} \quad V_{(\text{drop-twisted-4 runs})} = \frac{0.425 + 0.125}{4} = 0.1375 \text{ V}$$

The goal of 100 mV is still out of reach, especially when we consider that the power supply will contribute additional transient voltage drop in response to the change in output current. More specialized cabling options such as custom coaxial cables or flat wire cables can improve the inductance effect to as low as 10 nH/ft, however these options are costly and not as readily available. This leads us to the need for low-impedance energy storage located very closely to the test board.

## Using a Local Bypass Capacitor

The power supply is unable to compensate for the voltage drop across load leads as well as the drop across its own output rapidly enough, so you need a local source of energy, as shown in Figure 2. Capacitors are well suited to provide low impedance at high frequency to complement the low impedance provided at low frequencies by the power supply. Many different capacitor technologies are available, and finding the right part or combination of parts can be difficult. Ceramic capacitors are well suited for providing high-frequency bypassing at low voltages. However, even with the recent advances in ceramic capacitor technologies, they cannot match the high density and low price of aluminum electrolytic and conductive polymer aluminum solid electrolytic capacitors. The equivalent series resistance of the bypass network is an important parameter since it appears in series with the capacitor and can significantly reduce the effectiveness of the bypass network. Selecting the lowest necessary voltage capacitor will help you obtain the lowest-ESR capacitor and the highest capacitance density.

The interaction between the power supply voltage control loop, the load lead network and the bypass capacitance can be a bit complex. However, some useful approximations can help you with the initial value selection for the capacitor. The process:

### 1. Calculate peak network impedance

Determine the desired peak impedance of the load lead network and bypass capacitance by using the following expression:

$$\text{Eq. 6} \quad Z_{\text{peak}} = \frac{\text{Maximum desired voltage undershoot (V)}}{\text{Current transient amplitude (A)}} = \frac{100 \text{ mV}}{5 \text{ A}} = 20 \text{ m}\Omega$$

### 2. Calculate bypass capacitance value

Set the desired peak impedance equal to the expression for the characteristic impedance of the L-C tank formed by the load lead inductance and the bypass capacitance. Solve the expression for the value of capacitance,

$$\text{Eq. 7} \quad Z_{\text{peak}} = Z_c = \sqrt{\frac{\text{Load lead inductance (H)}}{\text{Bypass capacitance (F)}}} \rightarrow 20 \text{ m}\Omega = \sqrt{\frac{5 \times 170 \text{ nH}}{C}} \rightarrow C = 530 \mu\text{F}$$

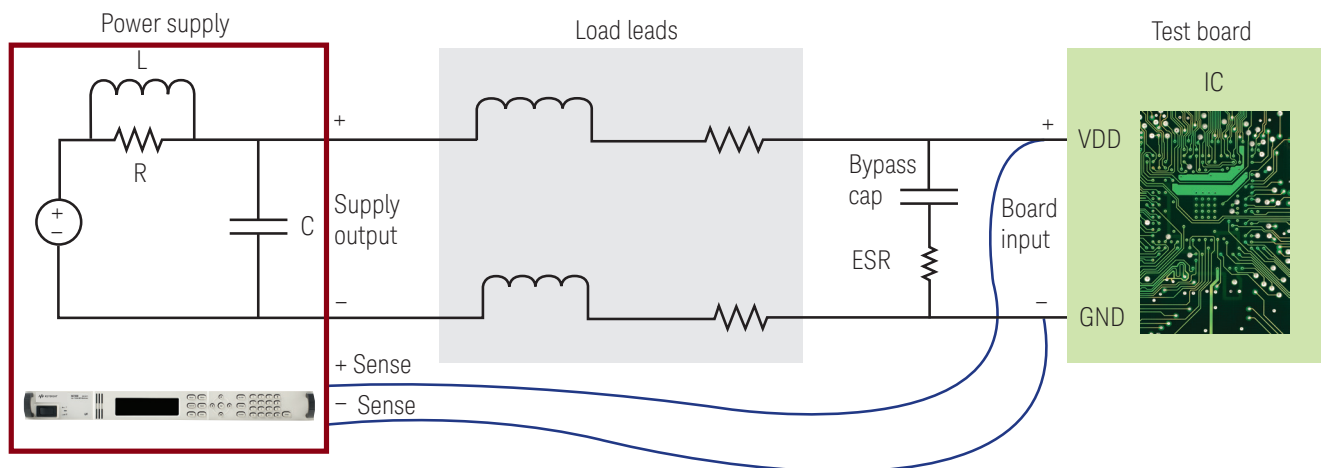


Figure 2. Load lead network with bypass capacitance

## Bypass Calculation (continued)

### 3. Calculate the resonant frequency of the tank

The power supply you use must have lower output impedance than the characteristic impedance of the L-C tank, otherwise the calculation you perform will not properly predict system behavior. The power supply output impedance will decrease with decreasing frequency. In a case where the power supply output impedance is higher than the desired peak impedance, pick a tank resonant frequency to equal the frequency at which the power supply output impedance is less than or equal to  $Z_{peak}$ . The resonant frequency will have to be lowered by selecting a larger bypass capacitor.

$$\text{Eq. 8} \quad F_{\text{resonance}} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{\frac{5 \times 170 \text{ nH}}{4} \times 530 \mu\text{F}}} = 15 \text{ kHz}$$

### 4. Select desired capacitor ESR to ensure proper damping of L-C tank

Proper damping of the resonant tank is crucial since an improperly damped tank will tend to ring and can also have a destabilizing effect on the power supply control loop. The combination of the load lead resistance and capacitor ESR will work to damp the resonant tank. We will target a damping ratio of 0.5 for faster response and lower peak voltage by equating the tank resistance to the L-C tank's characteristic impedance.

$$\text{Eq. 9} \quad Z_{\text{peak}} = \text{Load lead resistance} + \text{ESR} \rightarrow \text{ESR} = 20 \text{ m}\Omega - \frac{25 \text{ m}\Omega}{4} = 13.75 \text{ m}\Omega$$

Since it may not be possible to find one capacitor with the right capacitance and ESR, you can use parallel combinations of capacitors with different values and ESRs to arrive at the desired parameters.

## Results

Figure 3 shows the voltage transient response as observed at the load when using the Keysight Technologies, Inc. N7950A dynamic DC power supply. This unit is optimized for low voltage and high current operation and offers very low output impedance, which is ideal for this application.

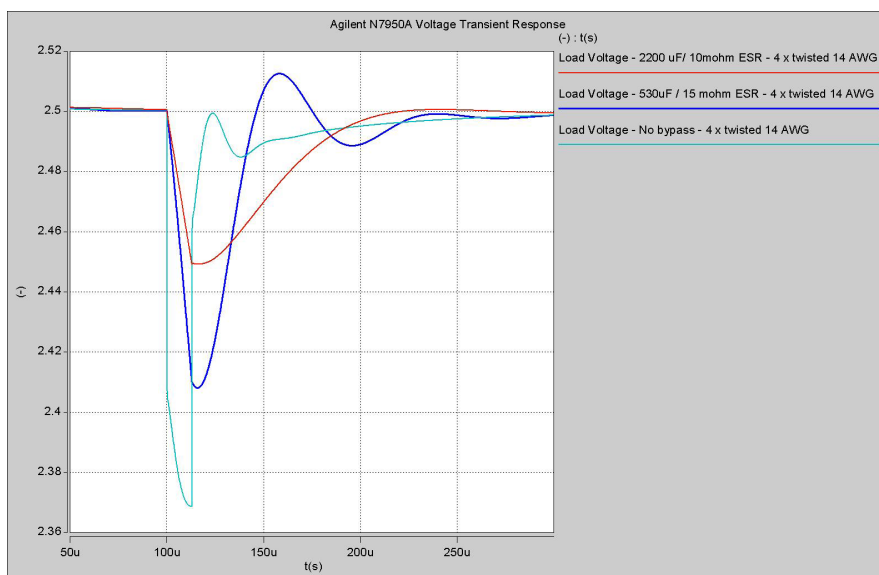


Figure 3. Voltage transient response to 5 A current transient

Two scenarios discussed in the example are shown, both using four runs, 5 feet long, each of twisted 14-AWG cabling, but one aided by the local bypass capacitor at the DUT. A third scenario is also shown. It uses four times more local bypass capacitance to drop the tank impedance by a factor of approximately two.

## Summary

In this application note we explored the challenge of supplying a highly dynamic load with a stable voltage using a power supply located several feet away from the device under test. Although the load lead impedance can severely degrade the transient response performance of a high-performance power supply, with the mitigation practices we discussed, you can achieve the required performance at the device under test. Techniques such as twisting load lead wiring to minimize the loop area formed between the supply and return lines, using flat copper, or heavy gauge coaxial cables can greatly reduce the load lead inductance. Properly sizing a bypass capacitor network at the device under test can further improve voltage level stability in the face of fast current transients drawn by the device under test.

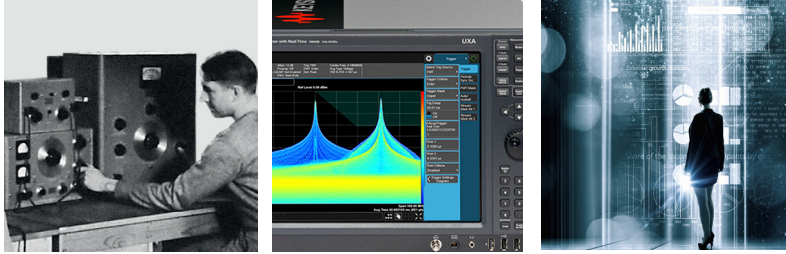
For more information on Keysight Advance Power System, kindly visits <http://www.keysight.com/find/N7900>



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